Data Sheet

iModeler:
Fast PDK Model Generation

A process design kit (PDK) is a set of files used within the semiconductor industry to model a fabrication process for the design tools used to design an integrated circuit. With a PDK, designers can jump-start chip design and work through the design flow seamlessly, from schematic entry to tapeout. PDK accuracy is essential for RFIC designs and increase the chances of first-pass successfully silicon. Cadence Virtuoso based schematic and layout flow is widely adopted for RF designs. iModeler allows PDK engineers to stay in Cadence Virtuoso design environment to easily create the parameterized cells (PCells), accurate parameterized equivalent circuit SPICE model, symbols and technology files. The fast 3D method of moments solver with both multi-core and distributed parallelization greatly reduces the EM simulation time thus improves PDK generation efficiency. Artificial Neural Network (ANN) based synthesis flow provides an efficient way to synthesize the passive components with +/-5% for 90% of samples, and greatly help IC designers to reduce the design cycles and achieve first-pass silicon success.

iModeler Solution

iModeler allows PDK engineers to stay inside Cadence Virtuoso to automate the PDK generation flow, including accurate PDK models, PCells, symbols and ANN based synthesis database. The built-in fast 3D full-wave solver yields both accuracy and efficiency advantages for PDK models. The rich set of built-in inductor, capacitor and transformer libraries help user to quickly build the useful templates.

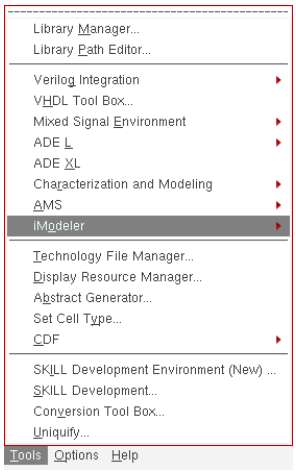
Key Points

- Accelerated 3D planar EM solver based on the Method of Moment (MoM) delivers the best performance in both speed and accuracy. It captures all the conductor and dielectric effects which are crucial for advanced nodes such as 45nm and below.
- Seamless integration with Cadence Virtuoso enables designers to stay in the Cadence design environment to perform the PDK creation flow.
- Support built-in PDK generation and synthesis wizard flow to easily create the parameterized cells (PCells), accurate parameterized equivalent circuit SPICE model, symbols and technology files.
- Support “PDK2Model” flow to quick create PDK accurate and parameterized models for existing PCells.
- Support several kinds of built-in templates to easy create PCells, including octagon/square inductor, MiM/MoM capacitor, resistor and interleave transformer.
- Artificial Neural Network (ANN) based synthesis flow provides an efficient way to synthesize the passive components with +/- 5% for 90% of samples.
- Support bias table and rho table in IRIS to account for technology variations for advanced IC nodes.
- Support set metal model and shielding option layer by layer based on metal thickness, width and spacing.
- Support multi-threading technology when build Green’s function to greatly improve the database creation efficiency and speed.
- Optimized mesh to balance speed and accuracy, support rectangle and triangle mixed mesh to improve simulation speed and convergence.
- Automatically disfeaturing via array when generate mesh file makes the geometry more EM-friendly.
- Support parallel processing techniques, including multi-threading processing and distributed processing to improve solver performance speedup and efficiency, and fully utilize hardware computing resources.
- SnpExpert provides powerful S-Parameter post-process capability.

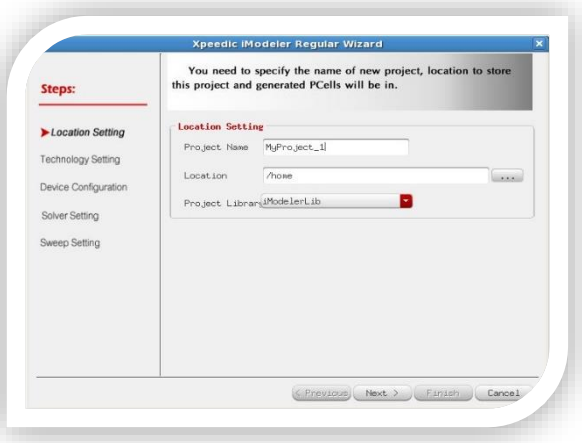
FEATURES

Design Environment

Xpeedic iModeler design flow is embedded in Cadence Virtuoso design environment. User needs to start Cadence Virtuoso first. In the 'Tools' pull down menu of CIW window, there is an 'iModeler' option, click it to start iModeler. Once iModeler is start up, the iModeler main window will pop-up, where the designer will deal with his projects.



CIW>Tools > iModeler



Design Wizard

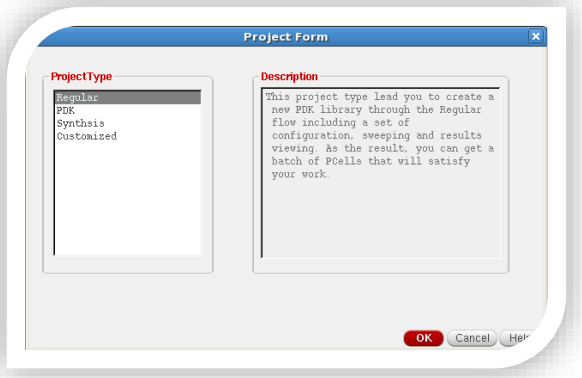
iModeler

Multiple Design Flow

Xpeedic iModeler provides several design flow: Regular, PDK, Synthesis and Customized. Regular is used to help design general devices like differential inductors, transformers, ect. PDK flow helps to verify devices in PDK with 3D EM simulation. In Synthesis flow, designers just need to give the device design goal and he will get one or more corresponding devices in return. Customized flow allows user to design any shape of device.

iModeler Menu

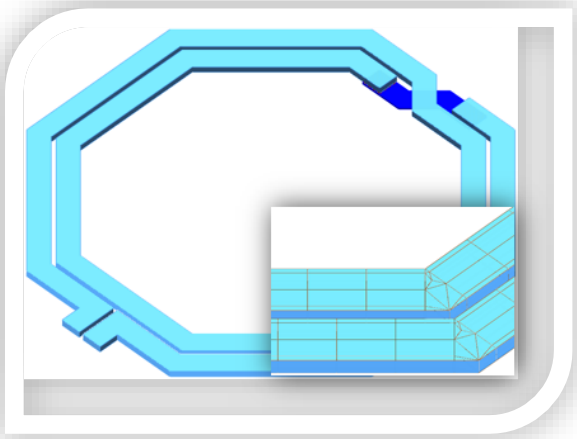
Xpeedic iModeler starts from selecting device type. By sweeping parameterized device, it returns a set of sweeping curves, according to which, user can create the corresponding cells in Cadence Virtuoso. A wizard leads the whole iModeler design flow. User can approach the flow step by step or skip it. The whole operations are in iModeler main window without importing or exporting files.



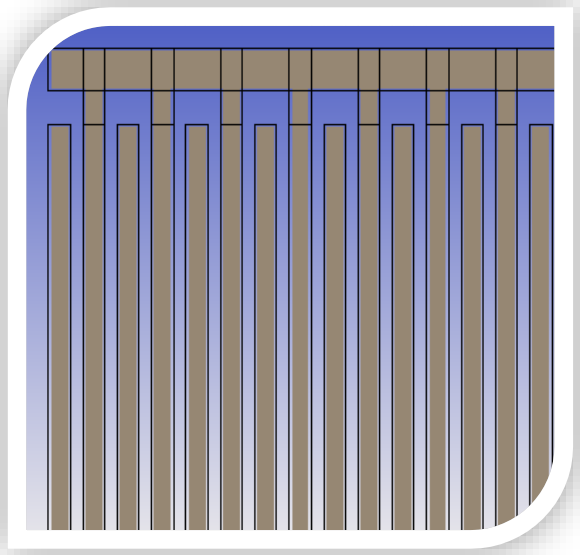
Select a Design Flow

Optimal Mesh Technology

iCell generated from Virtuoso layout for EM simulation use optimized mesh to balance speed and accuracy, iModeler mesher support rectangle and triangle mixed mesh to improve simulation speed and convergence. IRIS 3dview support 3D view of both layout structure and mesh.



Mesh View



Biased Mesh

3D EM Solver

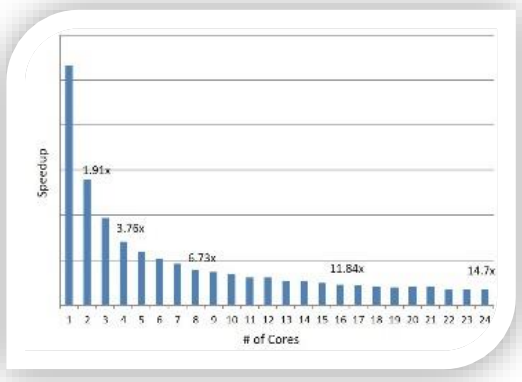
iModeler deploys a fast 3D full-wave Method-of-Moment (MoM) based EM solvers which delivers both speed and accuracy, and support 3D mode simulation to capture sidewall effect, and make it suitable for 45nm technology and below.

Advanced Technology Variation

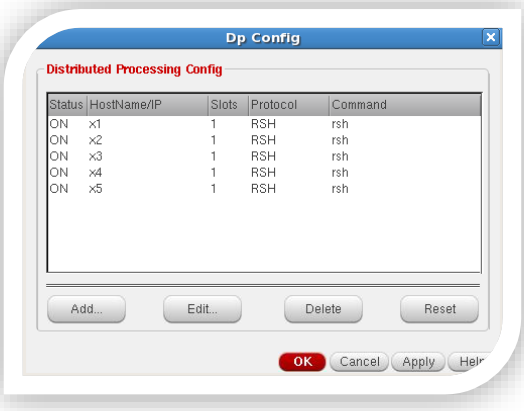
In advanced process technology, metal conductivity and width was not fixed since technology variation. iModeler support both rho table and bias table defined in process file to account for conductivity and geometry variation effect.

Parallel Processing Technique

In addition to the fast computation technology used in solver, iModeler also supports parallel processing technology to reduce simulation time. Both of distributed processing and multi-core processing are available, which can further increase the simulation efficiency with the update of computer hardware environment.



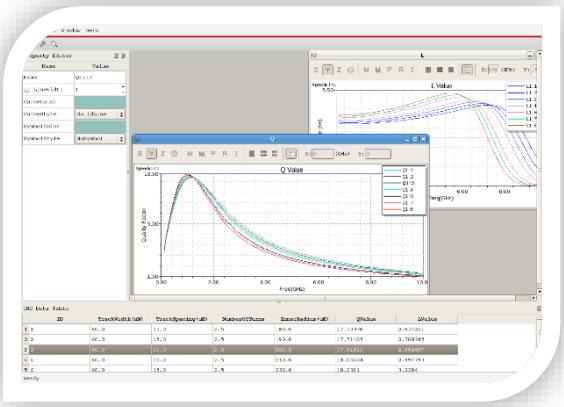
Multicore Speedup



Parallel Processing Option

Post Process

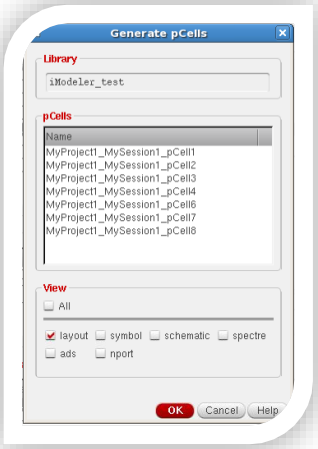
Once iModeler finishes simulation, user can get a set of sweeping resulting curves. With filter function, user can remove the useless curves. SnpExpert provides powerful S-parameter post-process capability. The template function enables user to plot by one click. Equivalent circuit model and broadband SPICE model can be exported in addition to S-parameter.



Waveform Display

Create Cell

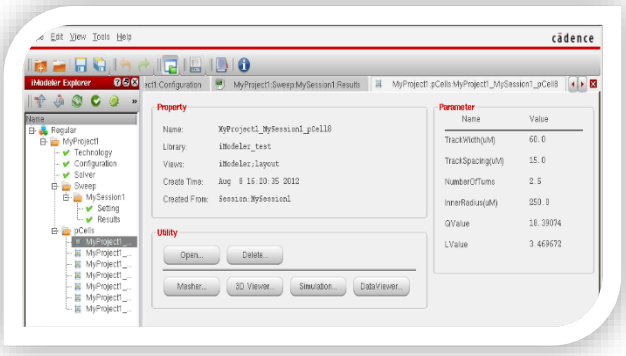
User can create corresponding cellviews (Symbol, Layout, ect.) of the resulting curves in Cadence Virtuoso.



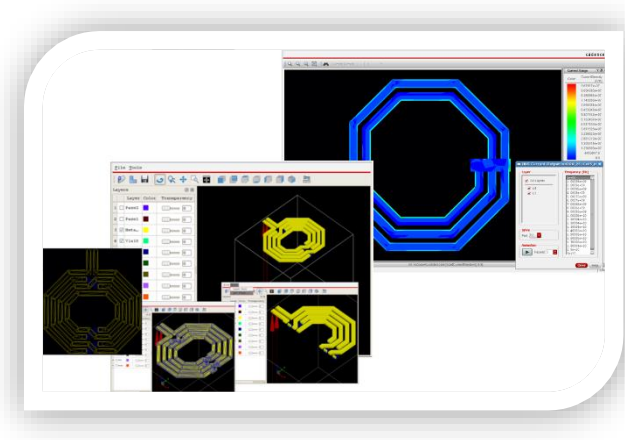
Generate Layout Cells

Device Information

Once a device is created, it will appear in the pCell item of the project tree. User can view device information by hit the name of the cell. Click'Mesh Viewer' and '3D Viewer'to check mesh and 3D structure of the device.



Browse Device Information



Visualized Plots

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