Data Sheet

iVerifier：

RF Passive PDK Verification

PDK model quality is essential for designers to design ICs with confidence. Typically PDK models are in the form of parameterized formula as function of physical parameters of the device, which are created via a mathematical data fitting process on either measured or simulated samples. The model quality is highly dependent on the number of samples and the number of terms in the fitted model. Xpeedic iVerifier provides a quick way to allow PDK engineers or IC designers to assess the PDK model quality by sweeping the model physical parameters and visualizing the model from various plots and tables. The built-in model templates offer designers an easy way to extract the electrical parameter from the model. The rich plot function allows designers to visualize the electrical parameters as function of physical parameters. Simply by examining the plots, the designers can assess the PDK model accuracy and the PDK completeness in terms of design space coverage.

Xpeedic iVerifier

Solution

Xpeedic iVerifier solution provides designers a quick way to verify PDK models in Cadence Virtuoso environment. It includes two flows, one is schematic based and the other is layout based. In iVerifier schematic flow, the PDK model test bench is run in ADE with Spectre simulator by sweeping the CDF parameters of the PDK model. In iVerifier layout flow, Xpeedic full-wave EM solver IRIS is run by sweeping the geometry parameters of PCell.

iVerifier provides a quick way to analyze and visualize the results, which helps PDK engineers or IC designers to assess the model quality.

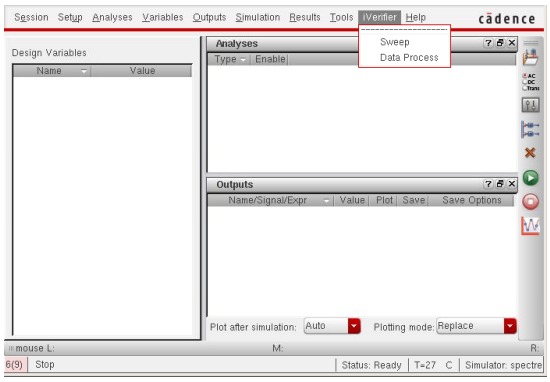
Key Points

- Seamless integration with Cadence Virtuoso.
- Easy definition of parametric sweeping.
- Both Spectre simulation and EM simulation can be activated. .
- Built-in template allows quick extraction of the electrical parameters.
- Multiple visualization plots helps to understand the impact on the electrical characteristics from the physical parameter sweep.

FEATURES

Design Environment

Xpeedic iVerifier is embedded in Cadence Virtuoso platform. It works for both schematic run with Spectre simulator and layout run with Xpeedic EM simulator IRIS. For the schematic flow, the iVerifier top menu can be found after launching ADE environment.



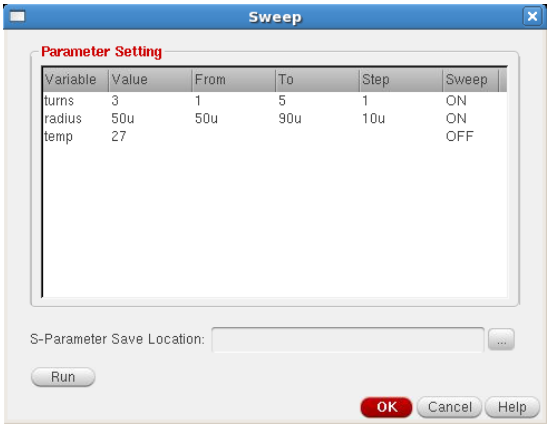
iVerifier Menu in ADE L/XL

For the layout flow, it can be found in Virtuoso Layout Suite XL Editing window.

iVerifier Menu in Cadence Virtuoso

Parametric Sweeping

For a given PDK device, Xpeedic iVerifier allows user to extract the physical parameters from the PCell and define parametric sweep easily.

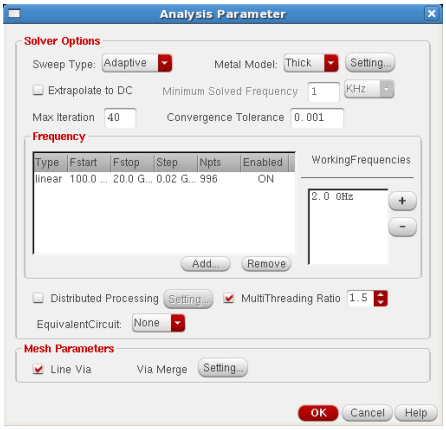


Parametric Sweep Setup

Fast EM Solver Technology

In layout flow, many EM simulations will be launched to cover the entire DOE table. The efficiency is highly dependent on the EM simulation speed. In iVerifier, this is achieved by using Xpeedic EM solver IRIS. Distributed

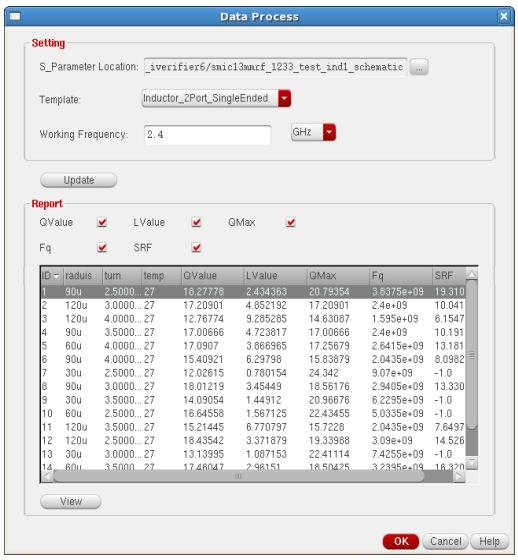
processing is also available for iVerifier.



EM Solver IRIS Setup

Data Process

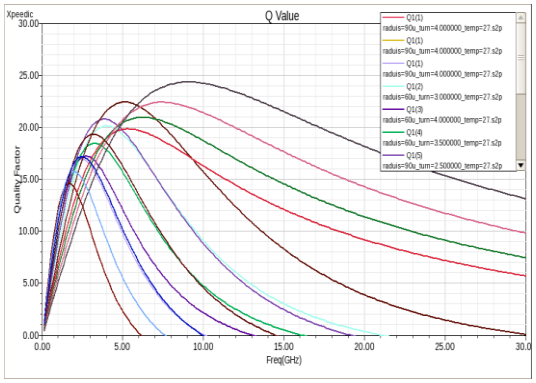
The large amount of data obtained from parametric sweeping are processed through the built-in template function. The electrical parameters for the given PDK device can be easily generated in a table.



Data Process Window

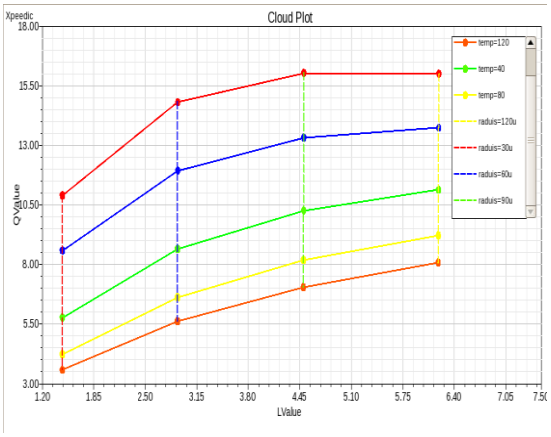
Data Analyze

Xpeedic SnpExpert provides multiple ways to visualize the data to understand the impact on the electrical characteristics from the physical parameter sweep. For example, multiple Q curves due to the number of turns sweep for an inductor case can be overlaid in one plot to help users to understand the relationship between number of turns and Q.



Sweeping Curves Sets in Frequency Domain

Other key parameters such as maximum Q or inductance value for an inductor case can be visualized in a contour plot.



Contour Plot

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