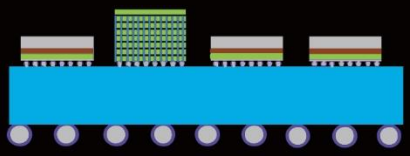
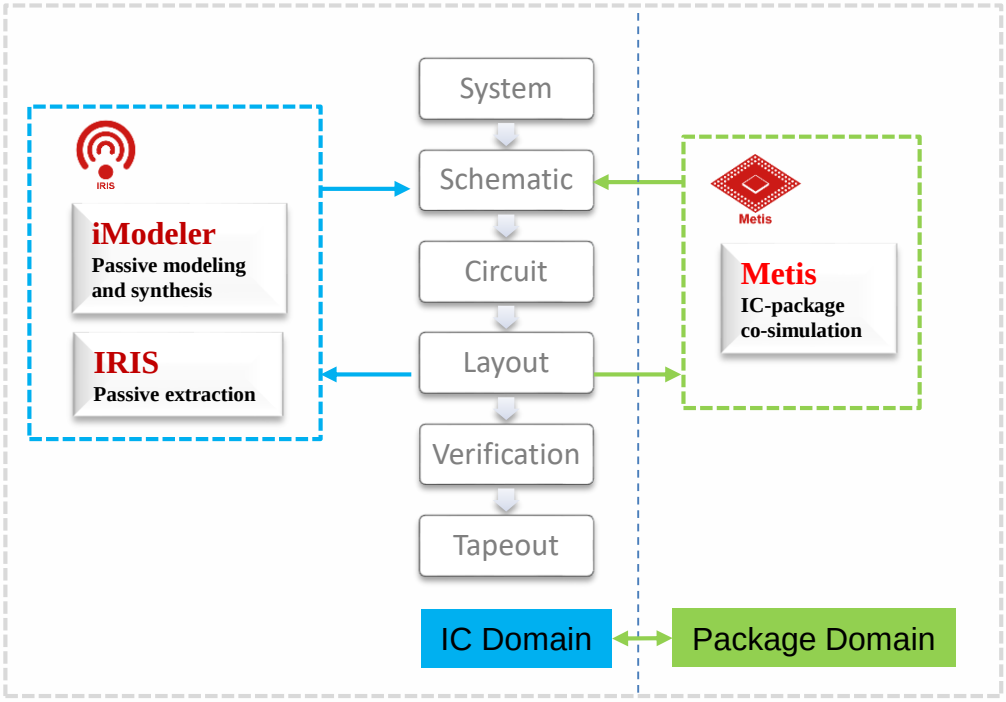


Using Metis for Fast IC-Package Co-simulation in RF IC Design

Highlights

1. RF front end (RFFE) has become more and more complex with evolving 5G wireless standard to support multiple bands, carrier aggregation, and MIMO.
2. System-in-Package (SiP) approach to integrate multiple dies and passives into one package is a viable solution to address the RFFE challenge.
3. However, IC design and package are typically divided efforts. Crossing the boundary is sometimes tedious and error-prone. Concurrent design can lead to reduced iteration and minimized error.
4. Enabling IC designers to assess the package effect anytime in their design flow is highly desired.
5. Metis offers a fast way to enable IC-package co-simulation. Not only it is easy to assemble the IC and package together for co-simulation, but also its state-of-the-art fast solver engine gives order of magnitude speedup compared to competitor solutions. Benchmark examples demonstrate the accuracy and speed of the Metis solver.

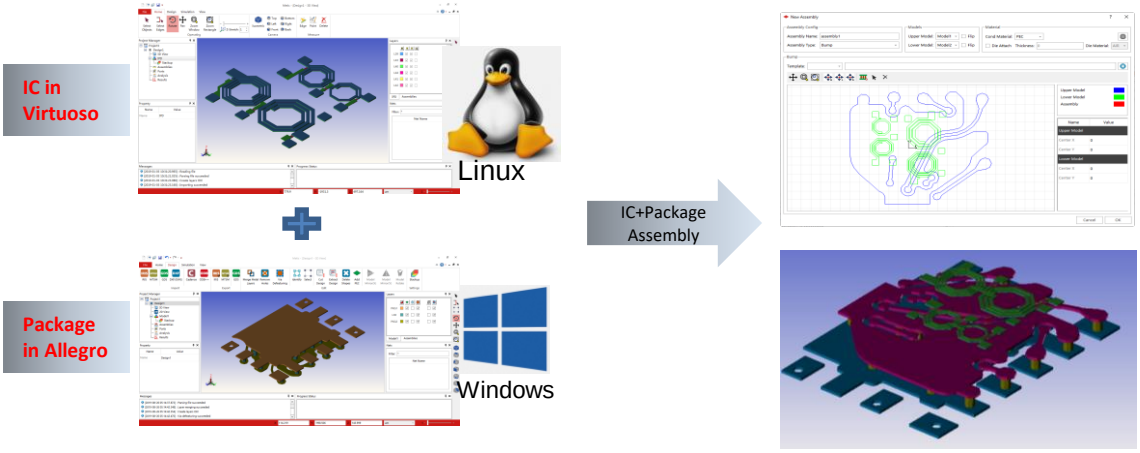
RF IC design flow with integrated EM simulation capability



- IRIS: state-of-the-art 3D planar EM simulator
  - Fast: Accelerated MoM technology, support both multi-core and distributed parallelization
  - Accurate: 3D conductor and via model, skin effect and proximity effect, full-wave from DC to THz
  - Certified in multiple foundry process nodes
- iModeler: fast passive modeling and synthesis
- Metis: fast IC-package co-simulation

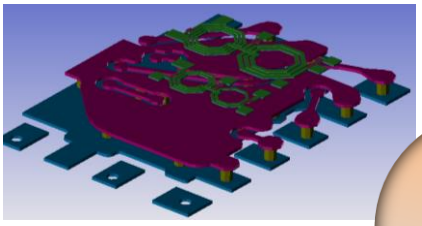
IC-Package Co-Simulation Example

- The IC-Package Co-simulation flow integrates IRIS, iModeler and Metis for analysis of IC/package coupling, signal integrity performance. Fast, easy to create wire bond or flip chip model 20x fast than conventional approaches, using accurate solver, to ensure engineer intent for signal quality is full achieved.



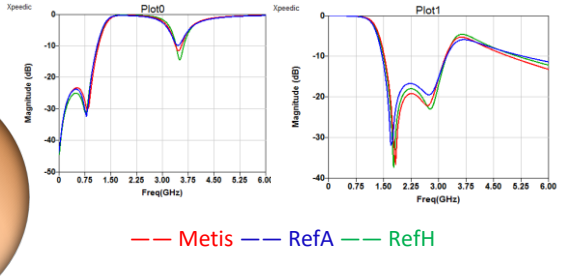
RF FEM in QFN Package

- The RF FEM simulation in QFN and BGA package enable rapid, full characterization of IC, die pad, bump, package pad for optimization and validation. Close integration with 3rd part tools for enhanced flexibility in FEM design.



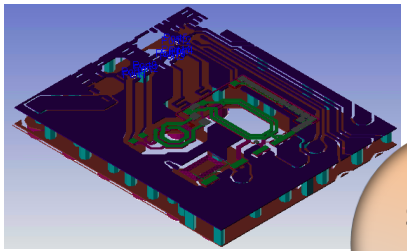
	Metis	RefA	RefH
Time	0.5 hr	4 hr	5 hr

Speed Up 10X



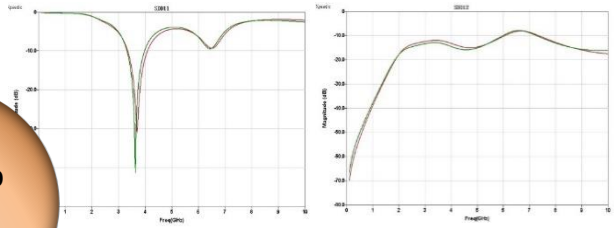
RF FEM in BGA Package

- The flexible and convenient RF FEM design flow with unique EM solver technology enable co-simulation of RF circuit blocks, multi-chip and multi-technology modules.



	Metis	RefH
Time	7.5 hr	64 hr

Speed Up 8.5X



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