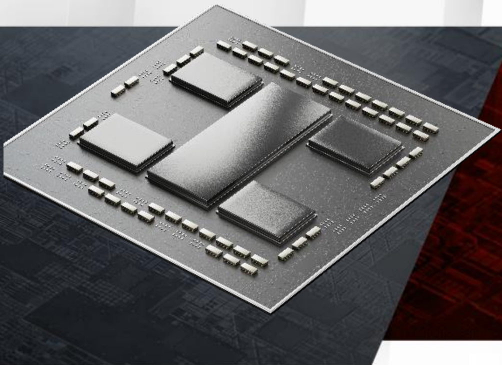
XPEEDIC
ACCELERATE YOUR IC DESIGN



2.5D/3D IC Chiplet Design with Advanced Packaging

Highlights

1

While Moore's Law continues driving transistor scaling, heterogeneous integration enabled by 2.5D silicon interposer and HBM becomes the norm for next generation HPC applications.

2

Silicon interposer with RDL and Through-Silicon-Via (TSV) sitting between IC and package requires cross-domain solution to tackle the signal integrity (SI) problems.

3

Xpeedic provides multiple SI analysis tools for 2.5D silicon interposer and HBM applications.

4

TmlExpert helps designer to study transmission line configuration in pre-layout stage, microstrip vs stripline, SGS vs coplanar ground, line-spacing for target impedance, etc.

5

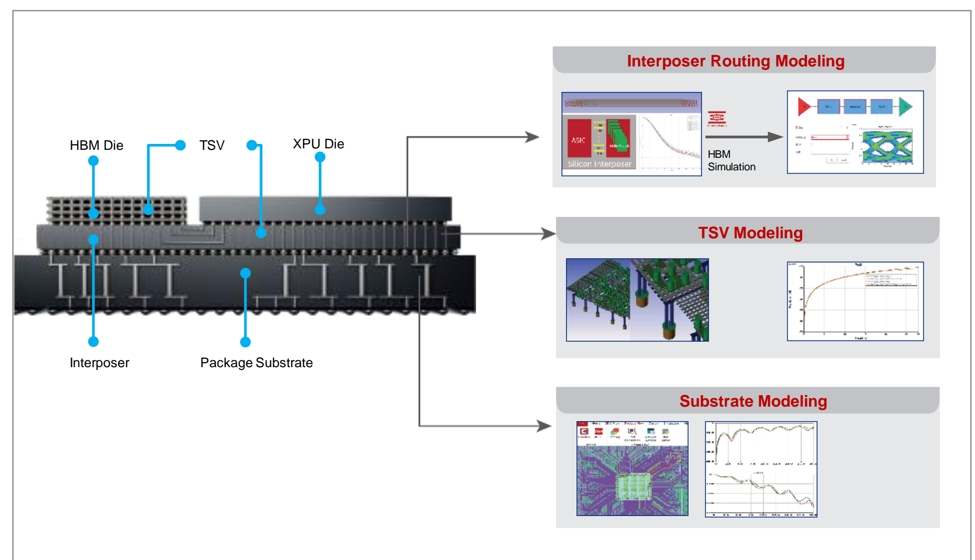
Metis accurately and efficiently extracts interconnect model for both HBM and die-package TSV channels.
Metis also provides transmission line and interposer template for pre-layout evaluation, which can help designer for quick pre-layout evaluation.

6

ChannelExpert helps designer torequickly build high-speed channel, run channel simulation, and check channel performance against compliance specs.

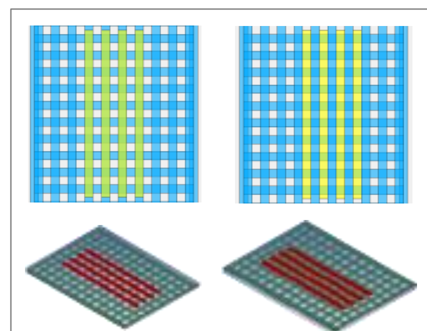
Xpeedic EDA Solution for 2.5D/3D IC Chiplet Design with Advanced Packaging

- Large-capacity EM solver to enable multi-die 2.5D/3D IC SI/PI analysis
- High-Speed Memory I/O Path: a large number of transmission lines on meshed ground plane need accurate and unified extraction for signal integrity.
- High-Speed Serial I/O Path: accurate TSV model is critical for signal integrity.



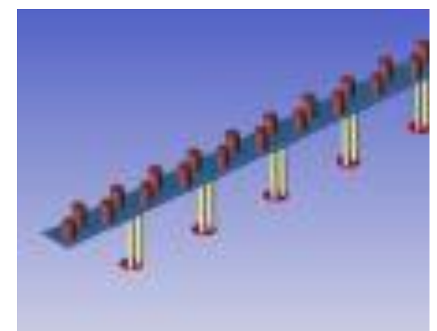
Transmission Line Design

TmlExpert has built-in interposer transmission line template to help designers to explore different configurations in terms of impedance, loss, delay, skew, and TDR.



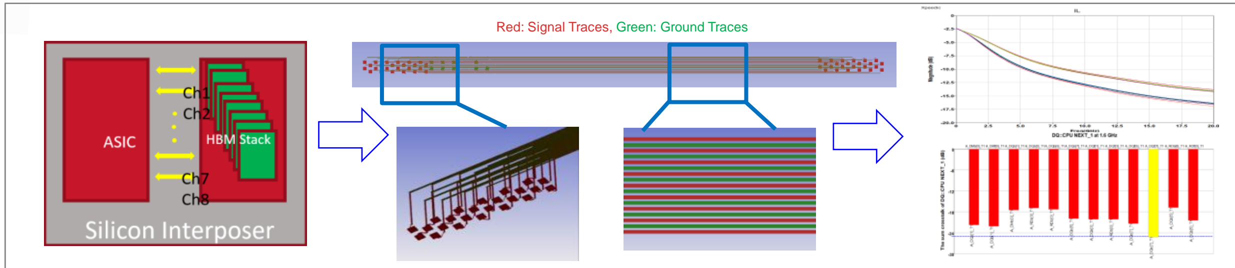
Interconnect Model Extraction

- Metis can extract interconnect model for both HBM and die-package TSV channels using one single solver without error-prone cut-and-stitch.
- It supports both GDS and ODB++ format.

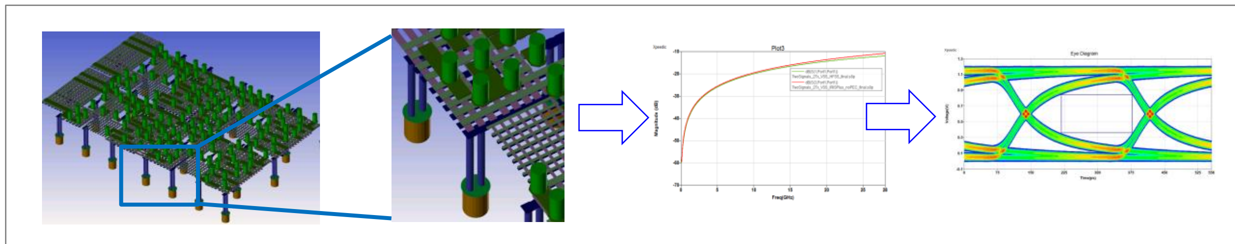


Interposer Signal Integrity Analysis

HBM signals are transmitted between ASIC die and HBM stack. Metis enables users to achieve interposer modeling by a wizard, which helps users simulate channel's loss and crosstalk between different dies accurately.

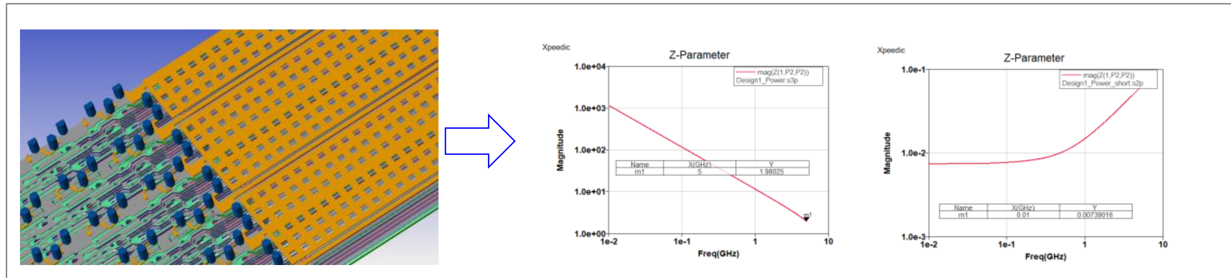


Die-package channel with TSV is critical for channel performance due to the loss and crosstalk introduced by the TSVs. Metis can accurately extract the model for the die-package channel.



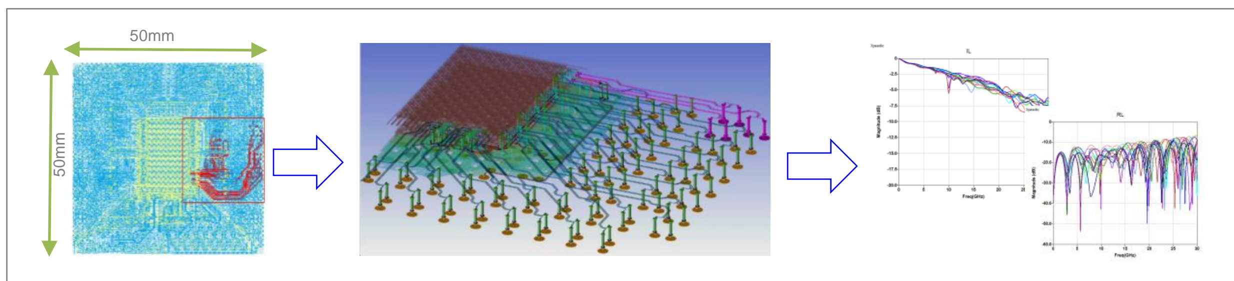
Interposer PDN Analysis

On the HBM interposer, significant numbers of I/O are integrated and they tend to operate at the same time which leads to severe simultaneous switching noise (SSN). When SSN occurs, the performance of system can be heavily degraded. The analysis of power distribution network (PDN) impedance of Chiplet/interposer must be performed since it generally affects power supply to the chips as well as signal integrity (SI).



Package/Substrate Modeling

For system SI and PI performance evaluation, transmission lines and power distribution networks on package substrate need accurate EM simulation. Metis provides a convenient simulation wizard for FCBGA package.



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