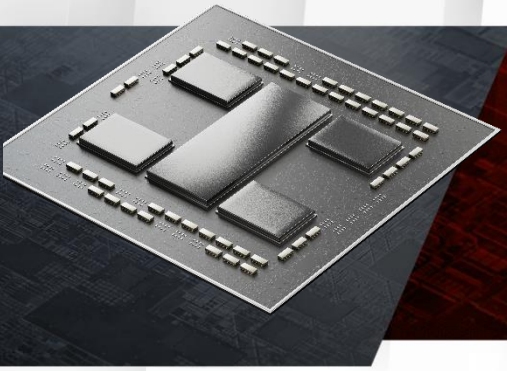


Metis

Large-capacity EM Simulation Platform for 2.5D/3D IC Chiplet Design

Highlights

1

While Moore's Law continues driving transistor scaling, heterogeneous integration enabled by 2.5D silicon interposer and HBM becomes the norm for next generation HPC applications.

2

Silicon interposer with RDL and Through-Silicon-Via (TSV) sitting between IC and package requires cross-domain solution to tackle the signal integrity (SI) problems.

3

Xpeedic provides multiple SI analysis tools for 2.5D silicon interposer and HBM applications.

4

Pre-simulation functions include Transmission-line characteristic impedance calculation, Pre-evaluation based on Interposer template; Transmission-line routing analysis based on customized transmission-line template and help designers to explore different configurations in terms of impedance, loss, delay, skew, crosstalk and TDR.

5

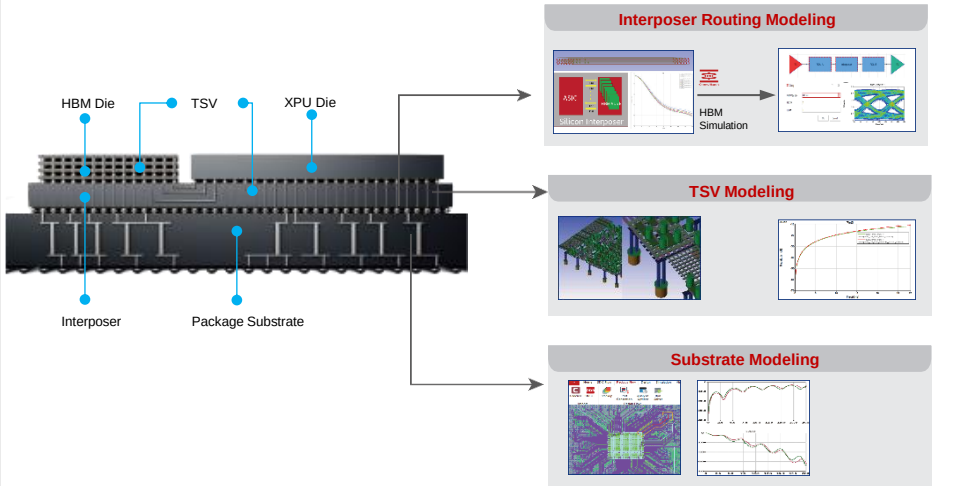
Metis accurately and efficiently extracts interconnect model for both HBM and die-package TSV channels.

6

ChannelExpert helps designer to quickly build high-speed channel, run channel simulation, and check channel performance against compliance specifications with models extracted by Metis.

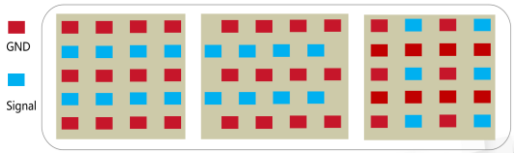
Xpeedic EDA Solution for 2.5D/3D IC Chiplet Design with Advanced Packaging

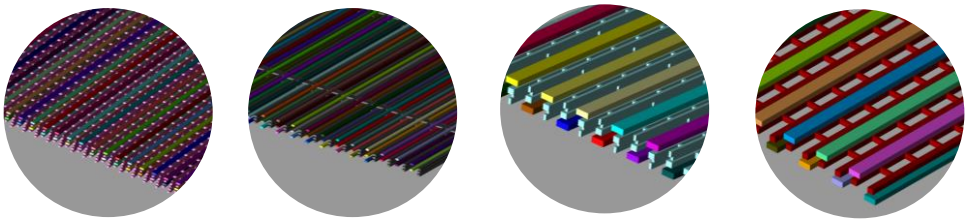
- Large-capacity EM solver to enable multi-die 2.5D/3D IC SI/PI analysis
- High-Speed Memory I/O Path: a large number of transmission lines on meshed ground plane need accurate and unified extraction for signal integrity.
- High-Speed Serial I/O Path: accurate TSV model is critical for signal integrity.



Pre-Layout Modeling and Simulation for RDL and Silicon Interposer

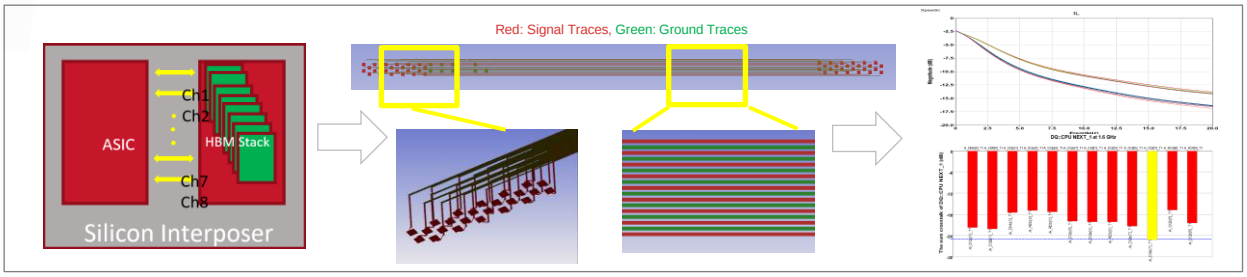
- Metis provides a 2D Interposer template to help users fast create RDL interposer design patterns for quick IL/RL/Xtalk evaluation.
- With the advanced silicon interposer pre-layout template, users can create RDL design patterns for CoWoS-S, and consider both trace and via characteristics for signal integrity.



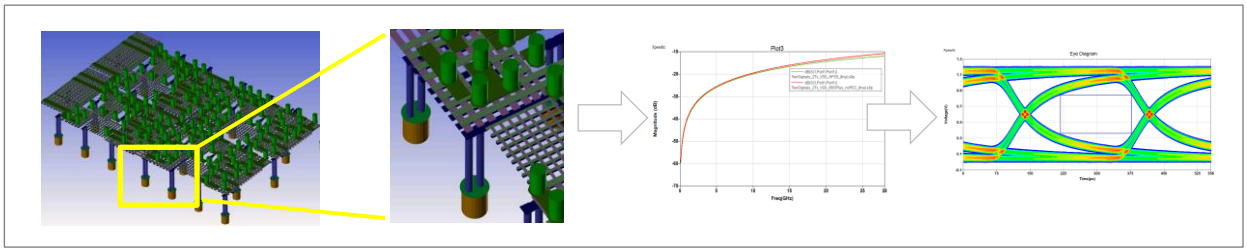


Interposer Signal Integrity Analysis

HBM signals are transmitted between ASIC die and HBM stack. Metis enables users to achieve interposer modeling by wizard for users to simulate channel's loss and crosstalk between different dies accurately.

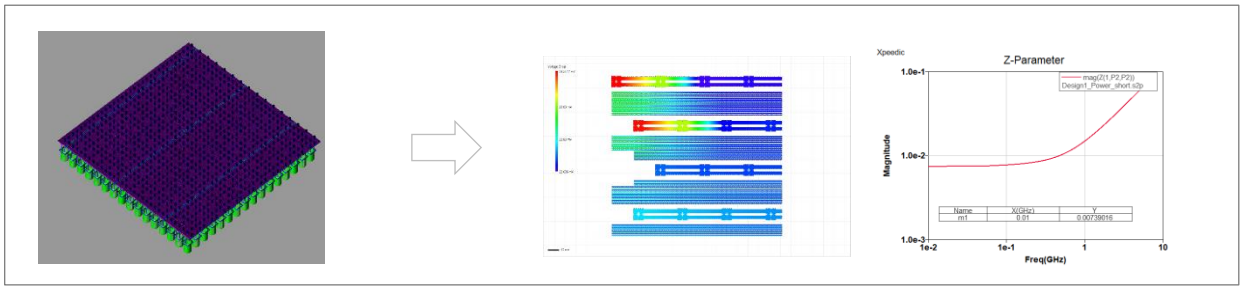


Die-package channel with TSV is critical for channel performance due to the loss and crosstalk introduced by the TSVs. Metis can well address it and extract the model accurately for the die-package channel.



Interposer PDN Analysis

On the silicon interposer, significant numbers of I/O are integrated and they tend to operate at the same time, which will lead to severe simultaneous switching noise (SSN). The performance of system can be heavily degraded when SSN occurs. The analysis of power distribution network (PDN) impedance and DC drop of Chiplet/interposer is a must since it generally affects power supply to the chips as well as signal integrity (SI).



Package/Substrate Modeling

For system SI and PI performance evaluation, transmission lines and power distribution networks on package substrate need accurate EM simulation. Metis provides a more convenient simulation wizard for FCBGA package.