

CHIP

CHIPLET

PACKAGE

SYSTEM

# Market Driver for Semiconductor Industry

The tectonic shift in computing from traditional PCs and smart phones to the Internet of Things (IoT) and cloud computing has brought explosive growth in data. Collection, storage, analysis and transmission of the massive data create vast opportunities for semiconductor industry.

Driven by the data economy, coupled with the continued commercialization of 5G and AI, emerging applications such as mobile communications, data centers, edge computing, and autonomous driving are reshaping the semiconductor industry landscape.

All these emerging applications demands SoC and system with better performance, power and area (PPA) and better integration, which in turn drives the innovation in every aspect of the semiconductor supply chain including process, packaging, system realizations and even design methodology to meet these demands.

# 2 Innovation In Semiconductor Industry

Semiconductor industry has been developing rapidly in accordance with Moore's Law for more than fifty years, providing the bonus of PPA (power, performance and area): reducing power consumption, enhancing performance and reducing costs. However, the advanced process is evolving towards 3nm and 2nm, and this trend is closing to the end with the physical limit.

Heterogeneous integration is a promising way to continue Moore's Law and can achieve the best PPA at the system level. The semiconductor industry is demanding more advanced technology in every aspect of its supply chain from IC design, foundry, packaging to final system.

### OPEN CHIPLET: PLATFORM ON A PACKAGE

# High-Speed Standardized Chip-to-Chip Interface (UCIe) - 20X I/O Performance at 1/20th Power vs offpackage SerDes at Launch - Gap more prominent with better on-package technologies in future Customer IP & Customized Chiplets Sea of Cores (heterogeneous) Memory Advanced 2D/2.5D/3D Packaging

# CHIP (

### **Advanced Nodes**

The process technology continues to evolve to 3nm and 2nm with Moore's Law.

# PACKAGE (+)

### **Advanced Packaging**

Heterogeneous integration which allows ICs from different processes, e.g. digital, analog, RF and MEMS, into a system-in-package delivers More-than-Moore. Advanced packaging technologies such as 2.5D interposer with TSV and 3DIC wafer level packaging are the recent examples in this wave of packaging technology development.

# SYSTEM (+

### **High Speed/Frequency**

5G mobile communications are shifting to higher frequencies and wider bandwidths, and the data transmission rate has increased to gigabit level. High speed serial/parallel link is ubiquitous to realize data processing, storage and transmission.

# 3 Challenges and Opportunities For EDA

All the aforementioned technology advances in IC, packaging, and system have posed great challenges to the EDA/IP industry. The traditional design methodology or even the underlying algorithm must be revised to meet the new demand arising from the new technology. Xpeedic was founded with this new requirement in mind and committed to offer the EDA/IP solution to better serve this rapidly growing market. Various advanced electromagnetic field solver technologies have been developed to tackle the specific challenges.



Metis provides powerful chip-interposerpackage co-simulation capability at the entire system level with innovative 2.5D/3DIC Chiplet advanced packaging solver technology.



Hermes provides efficient package-level signal integrity solutions with its innovative domain decomposition solver technology.



IRIS provides accurate EM modeling and simulation for passives and interconnects in advanced process nodes with unprecedented speed.



**Notus** adopts the most advanced hybrid electromagnetic algorithm and electrothermal coupling algorithm to solve SI/PI/Thermal challenges in 2.5D/3D multi-chip, packaging and circuit board design.



# Xpeedic Business Overview

Xpeedic's mission is to empower its customers with differentiating technologies to meet their ever-increasing challenges. Xpeedic is committed to keeping up with the latest technology progress and developing the best product to solve the application-specific problems.

# **EDA**

Xpeedic is a leading provider of EDA solutions to accelerate designs and simulations across chip, package and system levels for next generation high-frequency, high-speed intelligent electronic products. The product is backed with multiple home-grown proprietary solver technologies, covering both electro-magnetic and circuit simulation domains; Al-based mesh technology, supporting multi-scale simulation needs from nano-meter to centimeter level; advanced multi-core and multi-machine parallel computing technologies, realizing Xpeedic EDA cloud solution on AWS.



# **Xpeedic EDA Overview**

Simulation EDA from Chip to System



### Interconnection

System(Infrastructure/terminals, Data centers, Automotives), Connectors/cables/fibers and other arbitrary interconnection structures

3D full-wave EM simulation, Electrical performance post simulation



### **PCB**

PCB System (Infrastructure/terminals, High-performance computing and Storage, Network switching and routing)

Signal/Power Integrity, Multi-physics simulation including EM/Thermal/Stress analysis, System-level verification



### Module

RF devices/modules, Power devices, Optical modules, antennas, Decoupling capacitors design

Signal/Power Integrity, Multi-physics simulation including EM/Thermal/Stress analysis, System-level verification



### Package

Conventional/Advanced packaging (SiP, 2.5D/3D, Chiplet heterogeneous integration) design

Signal/Power Integrity design, Multi-physics simulation including EM/Thermal/Stress analysis

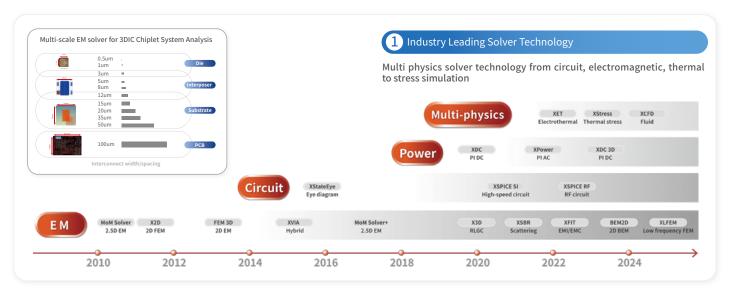


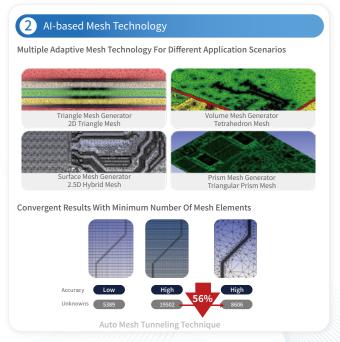
### Chip

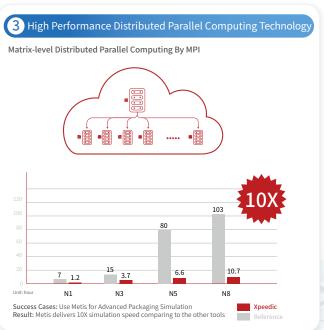
Analog/RF Chip Design on Silicon/ Compound Semiconductor Processes

Passive PDK generation, EM simulation, Spice circuit simulation, and Circuit-EM co-simulation

# **Xpeedic EDA Core Technologies**



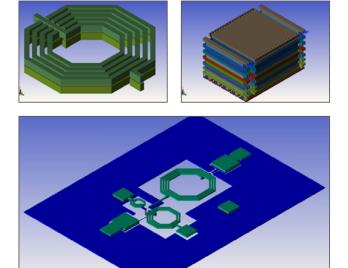


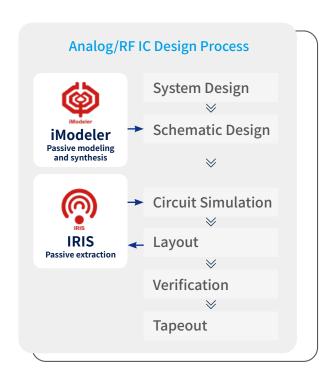


# **On-Chip Modeling for Advanced Process**

Accurate and fast EM simulation to enable RF and analog IC designs

\*IRIS: State-of-the-art 3D planar EM simulator \*iModeler: Fast passive component modeling and synthesis



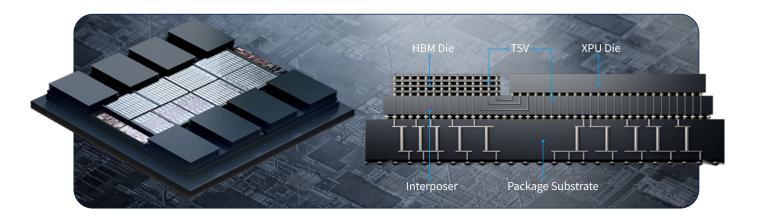


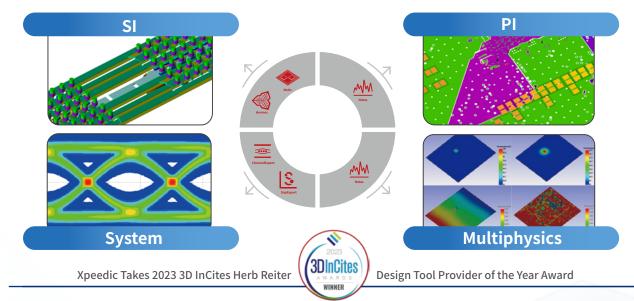
IRIS has been adopted by fabless on mainstream foundry nodes



# 2.5D/3DIC Chiplet Advanced Packaging

Large-capacity EM solver to enable multi-die 2.5D/3D IC Chiplet SI/PI analysis



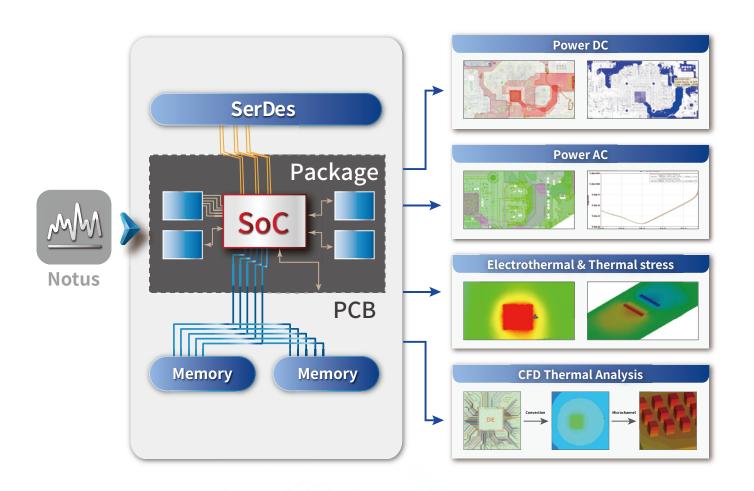


- 1 Multi-scale EM solver for 3DIC Chiplet System Analysis
- 2 AI-based Mesh Technology

- 3 High Performance Distributed Parallel Computing Technology
- 4 Support Die-Interposer-Substrate Co-Simulation

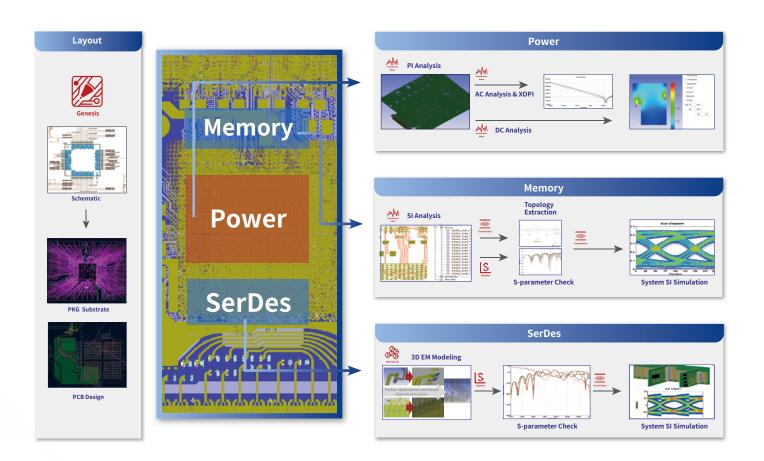
# **Multi-physics Simulation Platform**

Power integrity, Electrothermal, and Thermal stress multi-physics analysis



# High Speed Digital SI/PI Analysis

A comprehensive platform supporting high-speed serial/parallel interfaces

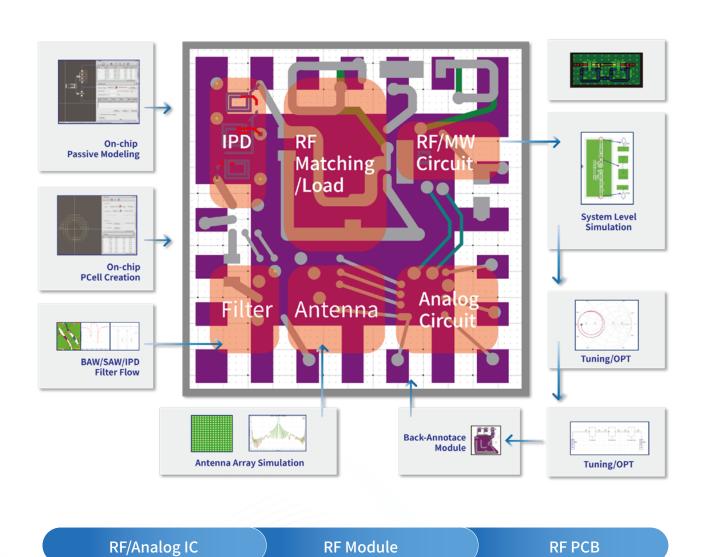


**Power Integrity** 

**Signal Integrity** 

# RF/Microwave System Analysis

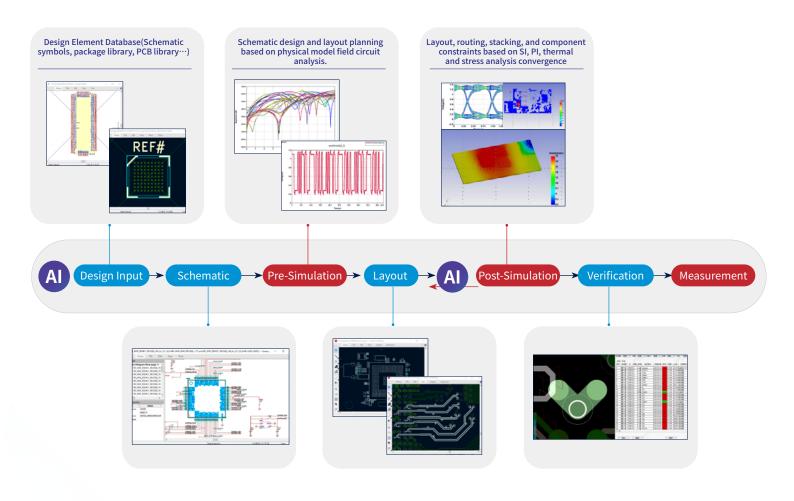
An integrated platform to support chip-package-module-board designs



9

# Package and PCB Design Platform

### Simulation-driven Design



- Simulation-driven PCB design to improve iteration efficiency, and has intelligent learning capabilities
- AI-empowered fully automatic or interactive routing mode

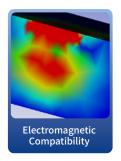
- Computing cloud support for collaborative design and distributed cloud computing technology
- Differentiated positioning supports efficiency improvement in automatic library construction, automatic layout, automatic routing

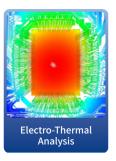
# **More Applications**

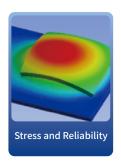
12 applications to accelerate electronic system design

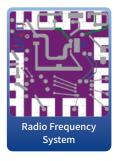




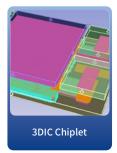




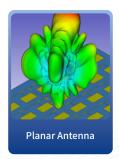




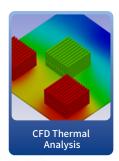












## **Product Family**

To enable next generation intelligent electronic system

### **Preliminary Modeling**

### **TmlExpert**

Transmission-line Modeling and Simulation

### ViaExpert

Via Modeling and Simulation

### CableExpert

Cable Harness Modeling and Simulation

### iModeler

Automated PDK Model Generation

### Layout Design

### **Genesis SCH**

Schematic Design

### **Genesis PKG**

Package Design

### **Genesis PCB**

PCB Design

### Genesis LIB

Automated Library Generation

### Multi-physics Simulation

### **IRIS**

Accurate and fast EM simulation to enable RF and analog IC designs

### Metis

Large-capacity EM solver to enable multi-die 2.5D/3D IC SI/PI analysis

### **Notus**

SI/PI/Thermal/Stress Simulation and Analysis

### **Hermes Layered**

3D FEM Simulation for IC/PKG/PCB

### Hermes 3D

3D FEM Simulation for Arbitrary 3D Structure and Antenna

### **Hermes Transient**

3D EM Compatibility Simulation

### X3D

Quick RLGC Extraction for Power/PKG/Touch Panel

### **XSBR**

3D Scattering Simulation

### Boreas

3D Fluid Simulation

### **System Verification**

### ChannelExpert

System SI/PI simulation platform for high-speed system

### **XDS**

RF / Microwave Circuit Design and Simulation

### Heracles

Automated Verification Kit for Highspeed Signal

### **Automated Measurement**

### SnpExpert

S-parameter Analysis Software

### MeasureExpert

Automated Measurement and Analysis

### **Cloud-based Management**

**XPLM** 

LicenseManager

**JobQueue** 

LibManager

Simulation Process and Data Management **Authorization Management** 

Simulation Job Queue System

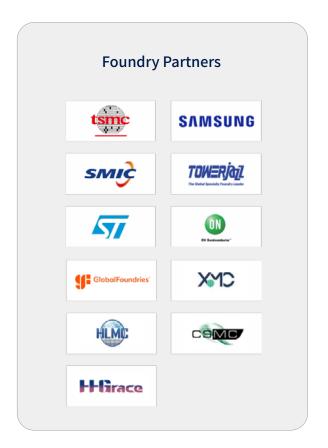
Library Management

# **Xpeedic EDA Ecosystem**

Connect design and manufacturing, providing comprehensive reliability, compatibility and usability











### **About Xpeedic**

Xpeedic is a leading EDA provider to accelerate designs and simulations of next generation high-frequency, high-speed intelligent electronic products. Powered by its proprietary electromagnetic, circuit, and multi-physics solver technologies, Xpeedic is addressing challenges in designing IC in advanced nodes, 3D-IC with advanced packaging, high-speed digital, and RF systems for the markets including data center, automotive, communication, mobile, and IoT.

Founded in 2010, Xpeedic has offices in both US and China. For more information, please visit www.xpeedic.com.

### **US Office**

19925 Stevens Creek Blvd #100 Cupertino, CA 95014

### **China Office**

60 Naxian Road, Bldg 5, Room 401, Pudong New Area, Shanghai, 201210

**Technical support** support@xpeedic.com

www.xpeedic.com