

## Simulation EDA From Chip to System

CHIP

CHIPLET

PACKAGE

SYSTEM

# Xpeedic EDA Overview

Simulation EDA from Chip to System



## System

Infrastructure/terminals, Data centers, Automotives

Multi-physics simulation including EM/Thermal/  
Stress analysis, System-level verification

## Interconnection

System(Infrastructure/terminals, Data centers, Automotives), Connectors/  
cables/fibers and other arbitrary interconnection structures

3D full-wave EM simulation, Electrical performance post simulation

## PCB

PCB System (Infrastructure/terminals, High-performance computing and Storage,  
Network switching and routing)

Signal/Power Integrity, Multi-physics simulation including EM/Thermal/Stress analysis,  
System-level verification

## Module

RF devices/modules, Power devices, Optical modules, antennas, Decoupling capacitors design

Signal/Power Integrity, Multi-physics simulation including EM/Thermal/Stress analysis,  
System-level verification

## Package

Conventional/Advanced packaging (SiP, 2.5D/3D, Chiplet heterogeneous integration) design

Signal/Power Integrity design, Multi-physics simulation including EM/Thermal/Stress analysis

## Chip

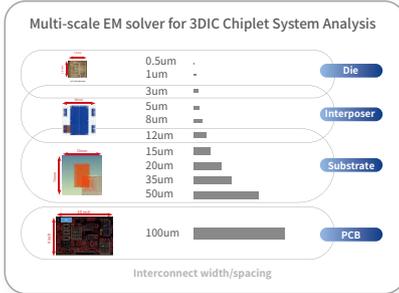
Analog/RF Chip Design on Silicon/ Compound Semiconductor Processes

Passive PDK generation, EM simulation, Spice circuit simulation, and Circuit-EM co-simulation

# Xpedic EDA Core Technologies

## 1 Industry Leading Solver Technology

Multi physics solver technology from circuit, electromagnetic, thermal to stress simulation



### Electro-magnetic

MoM Solver 2.5D EM, X2D 2D FEM, FEM 3D 3D EM, XVIA Hybrid, MoM Turbo 2.5D EM, X3D RLCG, XSBR Scattering, XFIT EM/EMC, BEM2D 2D BEM, XLFEM Low frequency FEM, MOM solver Lite 2.5D

### Circuit

XStateEye Eye diagram, XSPICE SI High-speed circuit, XSPICE RF RF circuit, XSPICE MS Power Supply Circuit

### Multi-physics

XET Electro-thermal, XStress Thermal-stress, XCFD Fluid, XStructure Structural stress

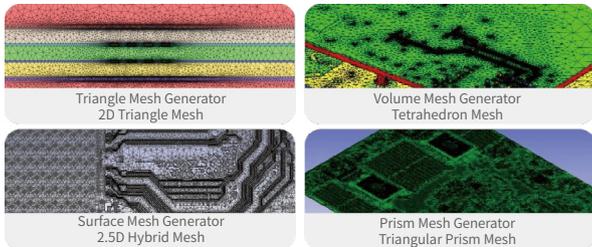
### Power

XDC PI DC, XPower PI AC, XDC 3D PI DC, X3DLite PI AC(3DIC)

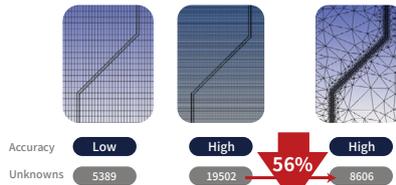


## 2 AI-based Mesh Technology

Multiple Adaptive Mesh Technology For Different Application Scenarios



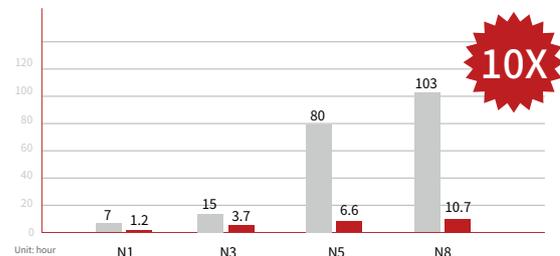
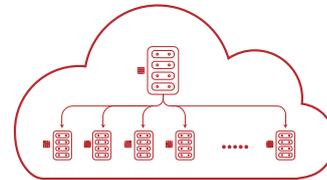
Convergent Results With Minimum Number Of Mesh Elements



Auto Mesh Tunneling Technique

## 3 High Performance Distributed Parallel Computing Technology

Matrix-level Distributed Parallel Computing By MPI



Success Cases: Use Metis for Advanced Packaging Simulation  
Result: Metis delivers 10X simulation speed comparing to the other tools

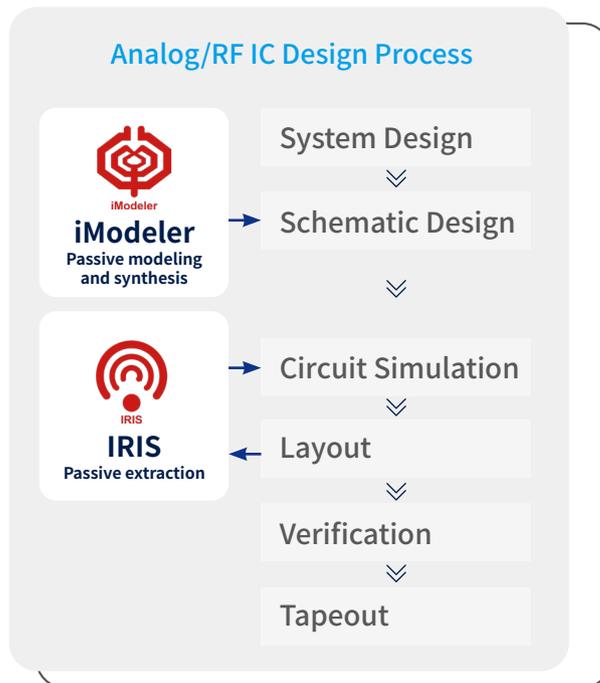
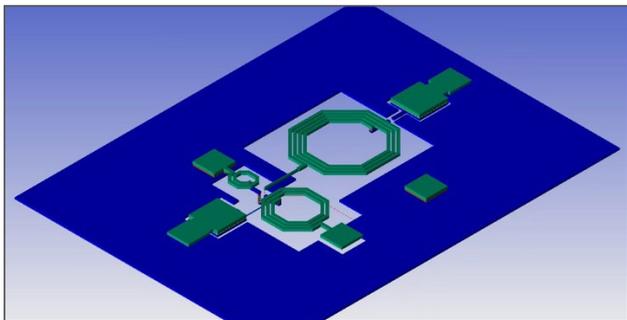
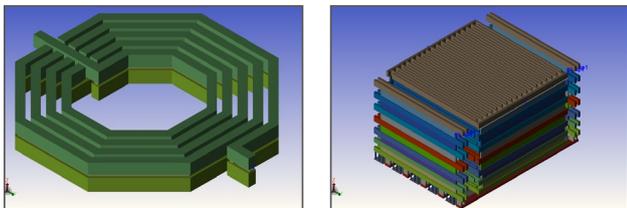
Xpedic Reference

## On-Chip Modeling for Advanced Process

Accurate and fast EM simulation to enable RF and analog IC designs

\*IRIS: State-of-the-art 3D planar EM simulator

\*iModeler: Fast passive component modeling and synthesis

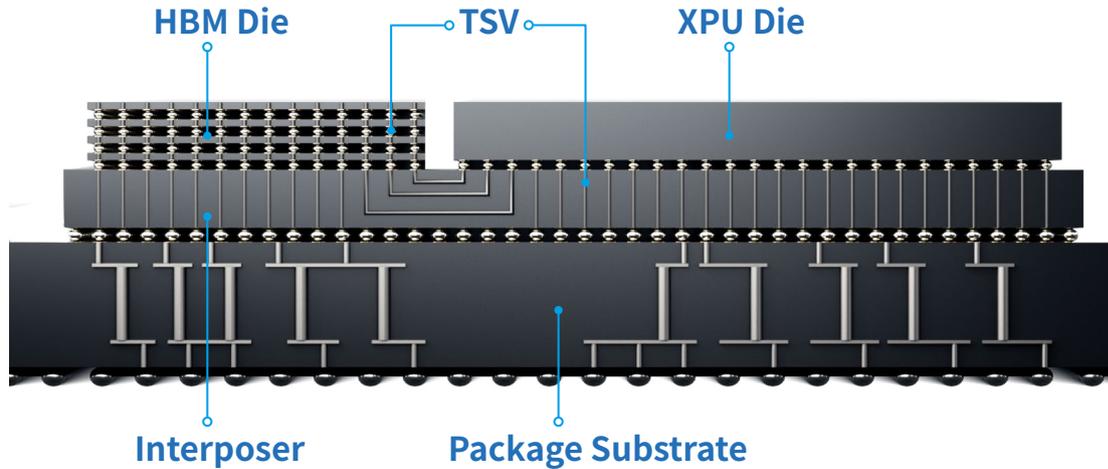


IRIS has been adopted by fabless on mainstream foundry nodes



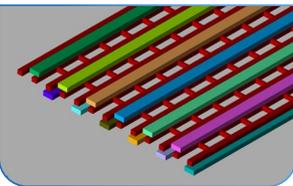
## 2.5D/3DIC Chiplet Advanced Packaging

Large-capacity EM solver to enable multi-die 2.5D/3D IC Chiplet SI/PI analysis



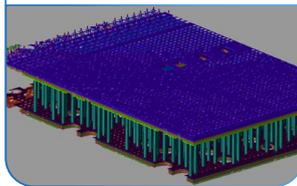
### Signal Integrity

- Support S-parameter extraction for signal and parasitic effect analysis
- Multi-scale co-simulation across chiplet-interposer-package



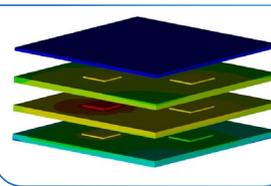
### Power Integrity

- Power delivery network DC IR-drop analysis
- Power delivery network AC impedance analysis



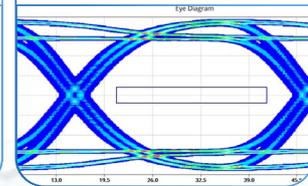
### Multi-physics Simulation

- EMI Analysis and Electromagnetic Coupling Effects Evaluation
- Electro-thermal and stress reliability analysis
- Multi-scale co-simulation across chiplet-interposer-package



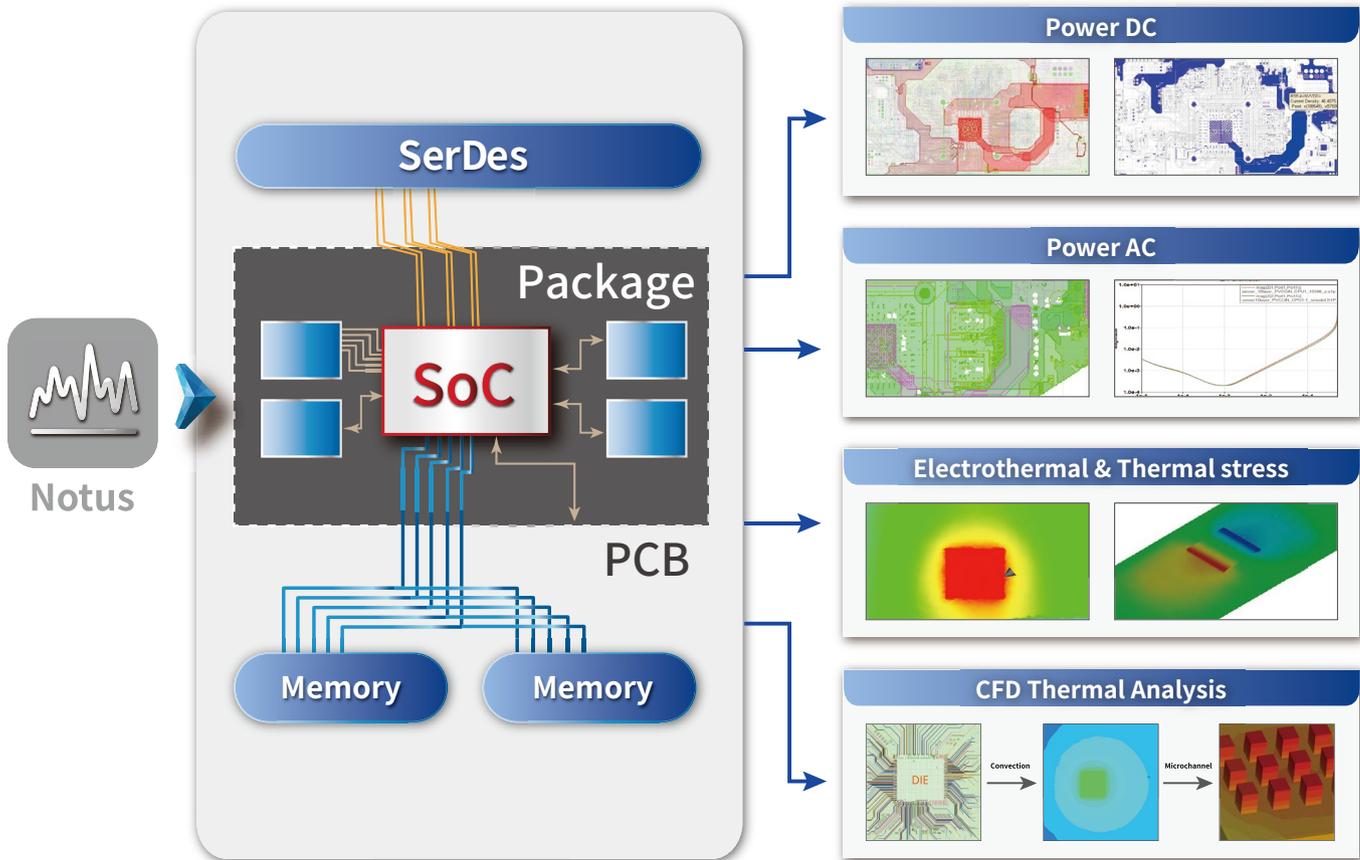
### System Verification

- High speed signal analysis and checking
- Post processing of simulated and measured data



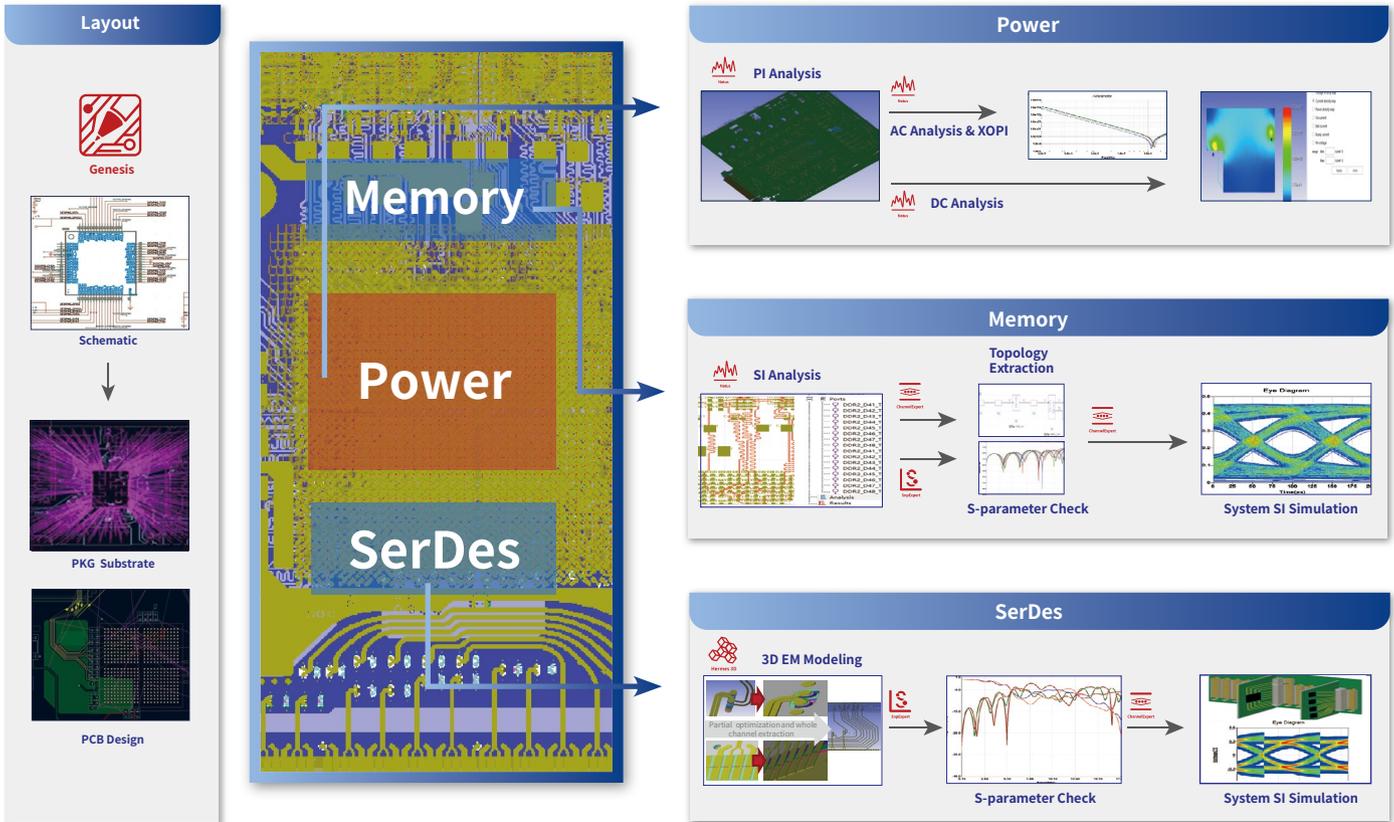
# Multi-physics Simulation Platform

Power integrity, Electrothermal, and Thermal stress multi-physics analysis



# High Speed Digital SI/PI Analysis

A comprehensive platform supporting high-speed serial/parallel interfaces



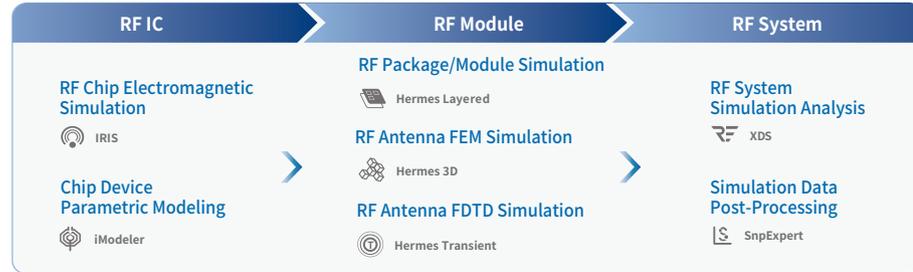
Power Integrity

Signal Integrity

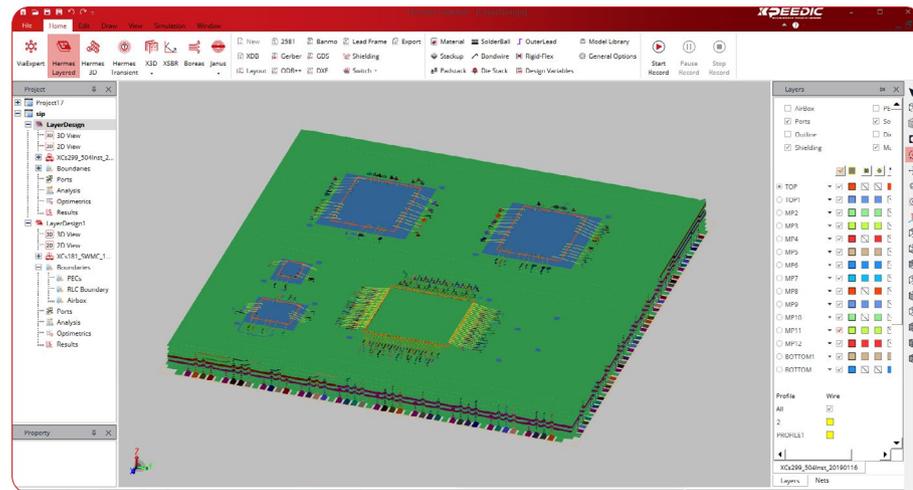
RF EDA solution from "chip, module to system", enabling RF system-level co-optimization

Key Features	Applications
<p><b>IRIS</b></p> <ul style="list-style-type: none"> <li>Seamless integrated with Virtuoso EM Simulation Flow for Integrated Passive Devices</li> </ul>	<p><b>Chip-Level</b></p> <p>RF IC Design</p>
<p><b>iModeler</b></p> <ul style="list-style-type: none"> <li>Passive device parametric templates and AI-powered high-accuracy modeling</li> </ul>	
<p><b>XDS</b></p> <ul style="list-style-type: none"> <li>RF module and system cross-scale field-circuit co-simulation with vendor model library integration</li> </ul>	<p><b>Module-Level</b></p> <p>RF Module/System Design</p>
<p><b>Hermes Layered</b></p> <ul style="list-style-type: none"> <li>Fast mmWave module modeling and adaptive mesh simulation</li> </ul>	
<p><b>Hermes 3D</b></p> <ul style="list-style-type: none"> <li>Full-scale antenna modeling DC-to-THz</li> <li>High-precision antenna near-field and far-field simulation analysis</li> </ul>	<p><b>System-Level</b></p> <p>Antenna Design &amp; Post-Processing Simulation</p>
<p><b>SnpExpert</b></p> <ul style="list-style-type: none"> <li>RF S-parameter visualization and electrical metrics</li> <li>Report generation and de-embedding /calibration</li> </ul>	

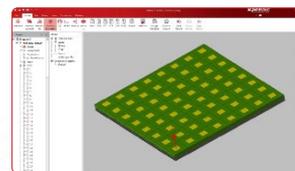
**Overview**



**Design Scenarios**



RF package EM simulation analysis



RF package layer 8x8 array antenna simulation analysis



RF IC passive interconnect network parasitic extraction

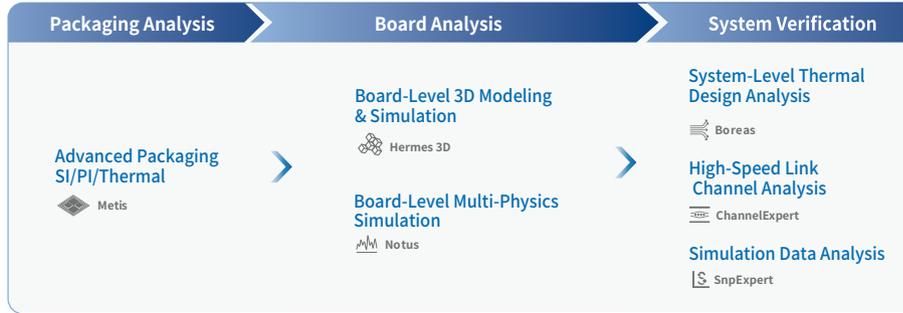


RF terminal system field-circuit modeling and co-simulation

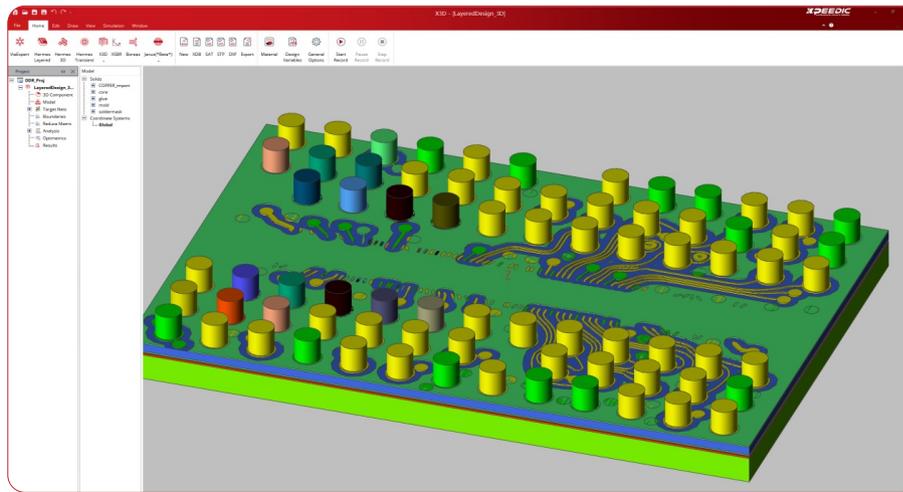
# Memory Solution

Memory EDA solution across chip–package–module–board–system

## ► Overview



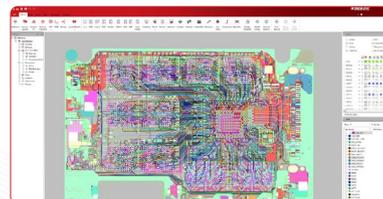
## ► Design Scenarios



DDR package modeling and simulation



DIMM SI/PI modeling and simulation



SSD board-level SI/PI modeling and simulation

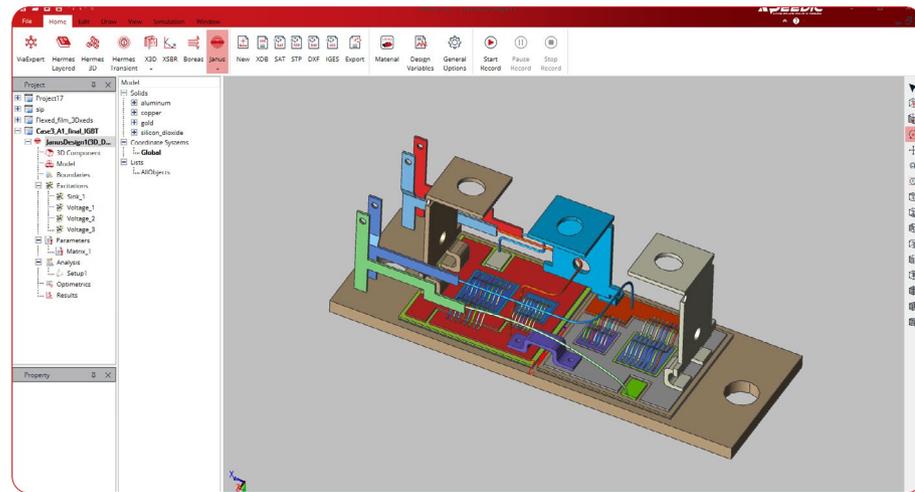
Applications	Key Features
Package-Level — Advanced Packaging and Module Design	<p><b>Metis</b></p> <ul style="list-style-type: none"> <li>Advanced packaging electro-thermal coupling analysis</li> </ul>
PCB System-Level — Mainboard and Expansion Board Design	<p><b>Hermes 3D</b></p> <ul style="list-style-type: none"> <li>Full-wave EM analysis for complex 3D package structures like multi-die stacking</li> </ul> <p><b>Notus</b></p> <ul style="list-style-type: none"> <li>Signal–power–thermal–stress simulation for memory packages/PCBs</li> </ul>
Memory Interconnect Structures — Connector and Cable Design Optimization	<p><b>Hermes 3D</b></p> <ul style="list-style-type: none"> <li>Modeling and analysis for various structural components like high-speed connectors</li> </ul> <p><b>CableExpert</b></p> <ul style="list-style-type: none"> <li>Modeling and analysis of high-speed memory extension cables</li> <li>Parametric design and frequency-domain modeling optimization</li> </ul>
Full Memory Link — Bus and Channel Simulation Verification	<p><b>ChannelExpert</b></p> <ul style="list-style-type: none"> <li>Eye diagram, jitter and BER analysis for DDR/HBM/PCIe channels</li> <li>JEDEC-compliant protocol model verification</li> </ul>

Power Device EDA Solution across chip-module-system for electrical performance, thermal management and reliability challenges

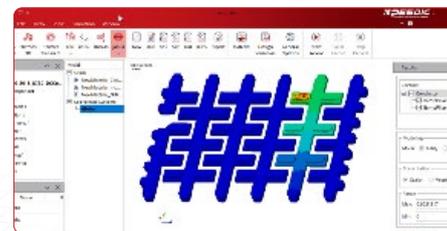
► Overview



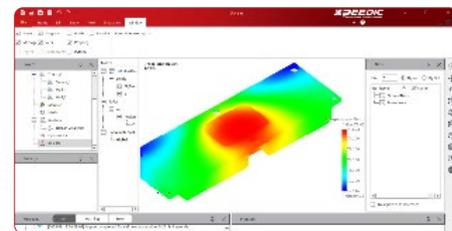
► Design Scenarios



IGBT module DC analysis



PDN Power Loss Analysis



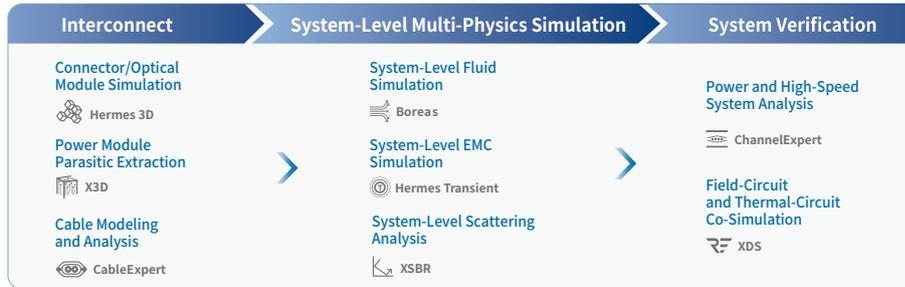
Server thermal module simulation

Key Features	Applications
<p><b>Janus</b></p> <ul style="list-style-type: none"> <li>DC and IR-drop analysis for power chip modules</li> </ul>	<p><b>Package-Level</b></p> <p>Power Chip-Level Device Module Design, DC Power Analysis &amp; Parameter Extraction</p>
<p><b>X3D</b></p> <ul style="list-style-type: none"> <li>Accurate R/L/C parasitic modeling for power devices and package interconnect structures</li> </ul>	<p><b>Package-Level</b></p> <p>Module Multi-Physics Simulation</p>
<p><b>Notus</b></p> <ul style="list-style-type: none"> <li>Multi-physics simulation platform for packages and power modules</li> <li>Electro-thermal-stress coupling analysis</li> </ul>	<p><b>Package-Level</b></p> <p>Module Multi-Physics Simulation</p>
<p><b>Boreas</b></p> <ul style="list-style-type: none"> <li>Board and rack-level thermal distribution simulation for multiple cooling solutions</li> <li>CFD thermal analysis for data centers and EV systems</li> </ul>	<p><b>System-Level</b></p> <p>Volume Thermal Analysis</p>

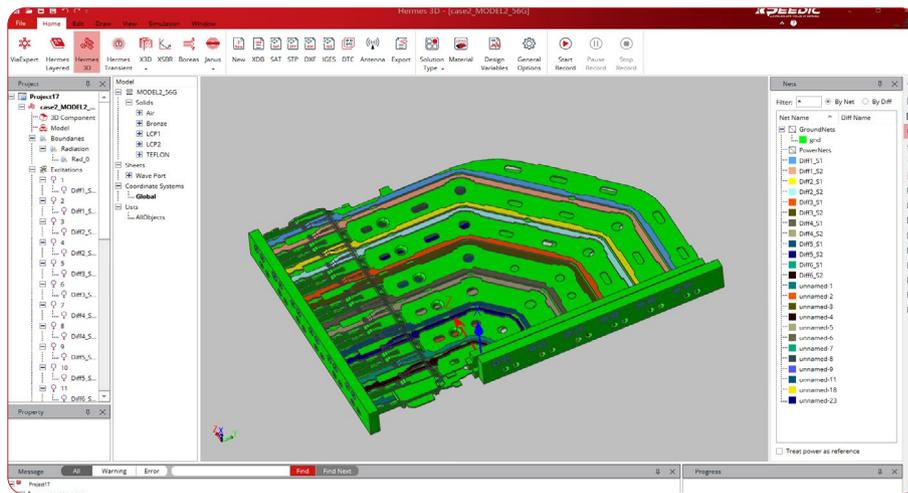
# Data Center Solution

Multi-physics co-simulation from Package, Board to System for data center challenges in high-speed interconnect, power delivery, and thermal management

## ► Overview



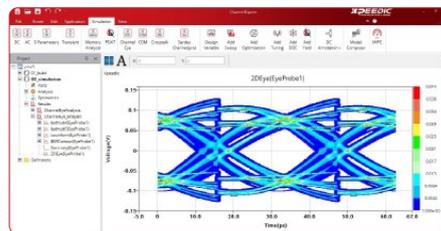
## ► Design Scenarios



High-speed connector modeling



High-speed cable modeling



PCIe 5.0 channel eye-diagram simulation

Applications	Key Features
PCB-Level Multi-Physics Analysis	<b>Notus</b> <ul style="list-style-type: none"> <li>Power stability evaluation and decoupling capacitor optimization</li> <li>Temperature monitor and thermal management</li> <li>High-speed circuit topology extraction and eye diagram analysis</li> </ul>
System-Level 3D EM Simulation	<b>Hermes 3D</b> <ul style="list-style-type: none"> <li>Full-structure 3D modeling, supporting simulation from DC to THz frequencies</li> </ul>
System-Level Parasitic Parameter Extraction	<b>X3D</b> <ul style="list-style-type: none"> <li>RLGC extraction for electronic system conductor structures from low to medium-high frequencies</li> </ul>
System-Level Next-Generation Digital System SI Analysis	<b>ChannelExpert</b> <ul style="list-style-type: none"> <li>High-speed channel frequency-domain S-parameter and time-domain eye diagram analysis (ChannelExpert)</li> <li>Accurate multi-model simulation and AMI modeling</li> </ul>
System-Level Next-Generation Cable Interconnect Architecture	<b>CableExpert</b> <ul style="list-style-type: none"> <li>Complex cable structures fast construction and custom topology design</li> </ul>
System-Level Electronic System Thermal Analysis	<b>Boreas</b> <ul style="list-style-type: none"> <li>Full-system CFD thermal analysis</li> </ul>

# Smart Terminal

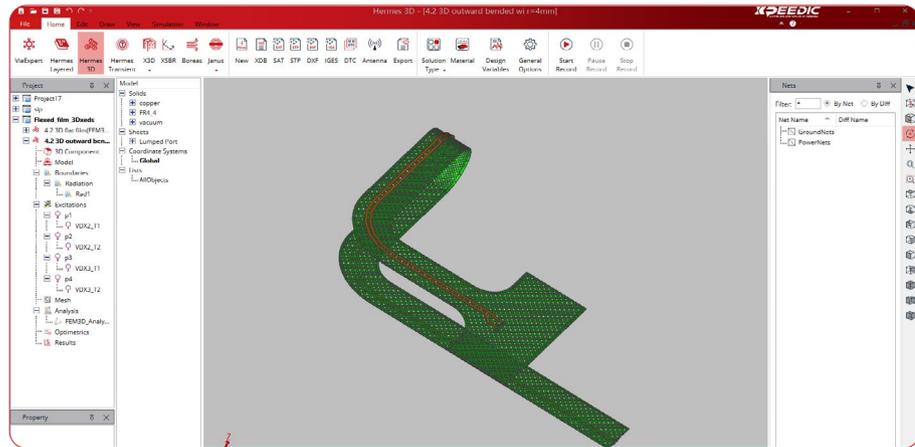
Solution

One-stop smart terminal solution, enabling simulation from chip, package, PCB to system verification

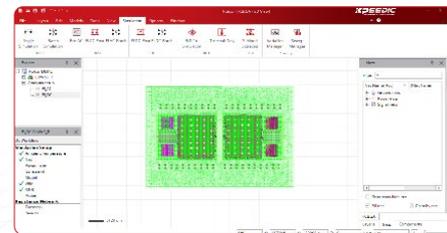
## Overview



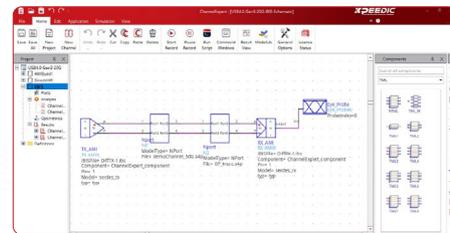
## Design Scenarios



Smart terminal flexible PCB simulation



High-performance AI-chip PI simulation

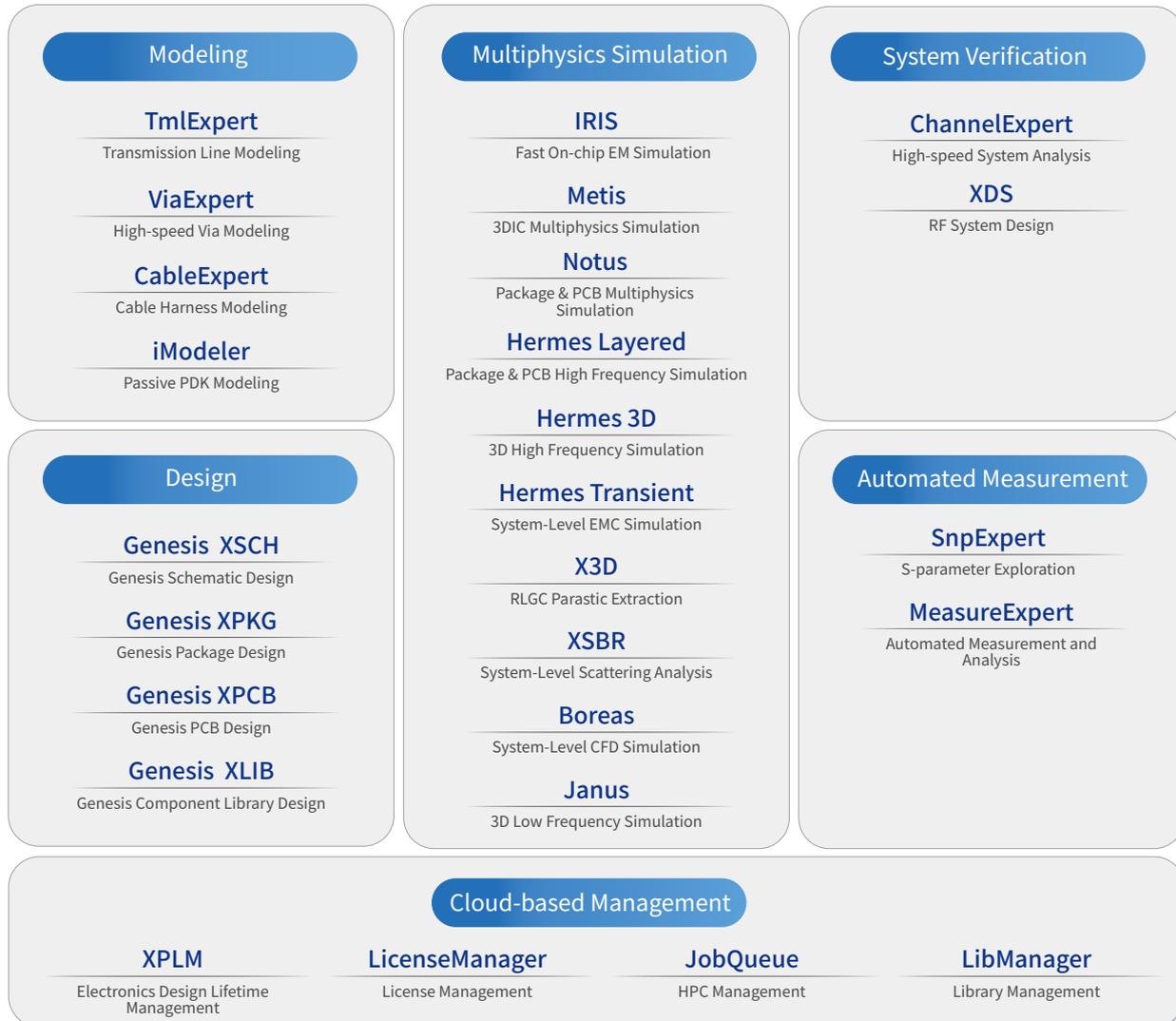


USB4.0 high-speed system verification

Key Features	Applications
<p><b>IRIS</b></p> <ul style="list-style-type: none"> <li>Full-wave EM analysis for SoC on-chip analog circuits and 5G RF circuits</li> </ul>	<p><b>Chip-Level</b></p> <p>Analog/RF Chip Design</p>
<p><b>Metis</b></p> <ul style="list-style-type: none"> <li>Chiplet interposer SI, PI, and thermal stress analysis</li> </ul>	<p><b>Package-Level</b></p> <p>2.5D/3D Advanced Packaging Interposer, Package Substrate, PCB Design</p>
<p><b>Hermes</b></p> <ul style="list-style-type: none"> <li>Low-voltage, high-current power integrity and thermal stress analysis</li> <li>Product reliability optimization under harsh environments</li> </ul> <p><b>Notus</b></p> <ul style="list-style-type: none"> <li>High-speed channel &amp; antenna radiation analysis</li> <li>Multi-physics coupling simulation</li> </ul>	<p><b>PCB Board-Level</b></p> <p>Package Substrate, PCB Multi-Physics Simulation Analysis</p>
<p><b>ChannelExpert</b></p> <ul style="list-style-type: none"> <li>High-speed channel system-level verification</li> <li>Reduce high-speed signal transmission distortion</li> </ul>	<p><b>System-Level Verification</b></p>

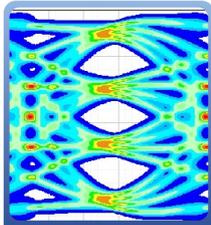
# Product Family

To enable next generation intelligent electronic system

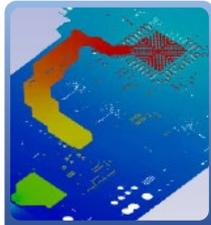


## More Applications

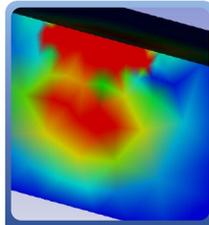
12 applications to accelerate electronic system design



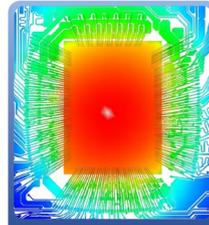
Signal Integrity



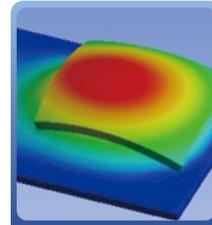
Power Integrity



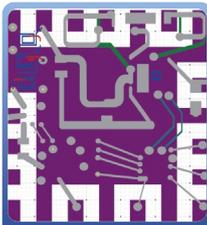
Electromagnetic  
Compatibility



Electro-Thermal  
Analysis



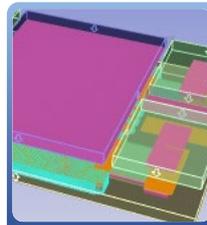
Stress and Reliability



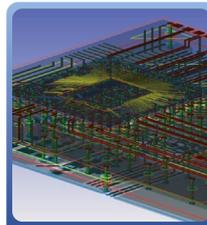
Radio Frequency  
System



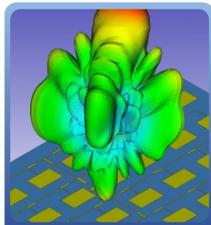
Package Substrate



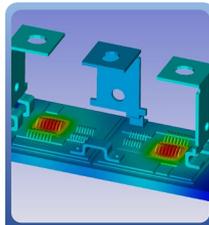
3DIC Chiplet



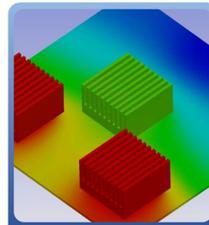
PCB Board



Planar Antenna



Power Semiconductor  
Device



CFD Thermal  
Analysis



## About Xpeedic

Xpeedic is a leading EDA provider to accelerate designs and simulations of next generation high-frequency, high-speed intelligent electronic products. Powered by its proprietary electromagnetic, circuit, and multi-physics solver technologies, Xpeedic is addressing challenges in designing IC in advanced nodes, 3D-IC with advanced packaging, high-speed digital, and RF systems for the markets including data center, automotive, communication, mobile, and IoT.

Founded in 2010, Xpeedic has offices in both US and China. For more information, please visit [www.xpeedic.com](http://www.xpeedic.com).

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