XPEEDIC
POWERING CHIP-TO-SYSTEM INTELLIGENCE

Metis

2.5D/3D IC Chiplet Design SI/PI/Thermal Simulation Platform

Highlights

1

While Moore's Law continues driving transistor scaling, heterogeneous integration enabled by 2.5D silicon interposer and HBM becomes the norm for next generation HPC applications.

2

Silicon interposer with RDL and Through-Silicon-Via (TSV) sitting between IC and package requires cross-domain solution to tackle the signal integrity (SI) problems.

3

Pre-simulation functions include Transmission-line characteristic impedance calculation, Pre-evaluation based on Interposer template; Transmission-line routing analysis based on customized transmission-line template and help designers to explore different configurations in terms of impedance, loss, delay, skew, crosstalk and TDR.

4

Metis accurately and efficiently extracts interconnect model for both HBM and die-package TSV channels.

5

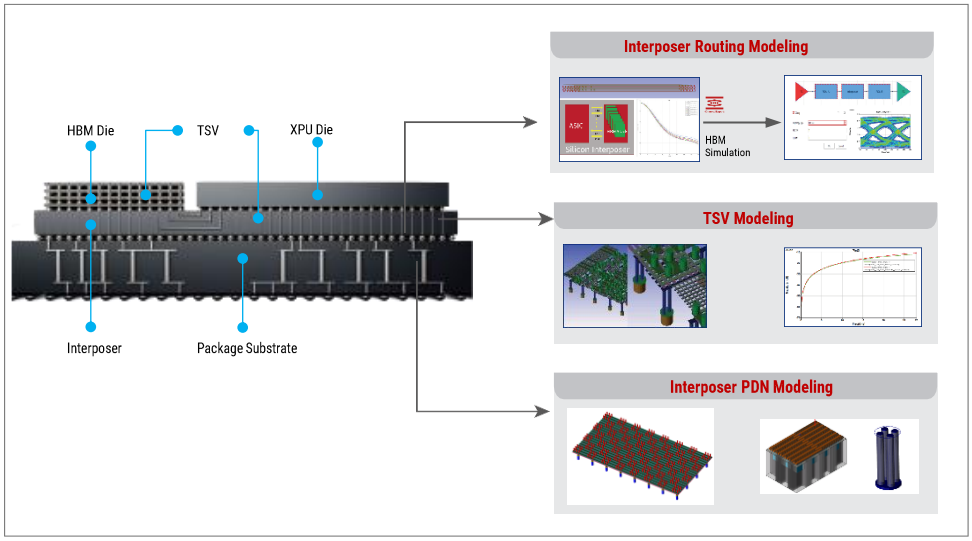
Metis provides the PDN DC analysis flow for interposer, enabling designers to accurately identify issues such as IR Drop and Current Density. The PDN AC analysis adopts quasi-static solving technology to precisely simulate DCR and high-frequency inductance.

6

AI Agent enables natural language requirement input, while Metis automates modeling and simulation to speed up design iterations.

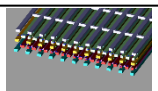
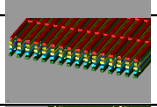
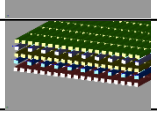
Xpeedic EDA Solution for 2.5D/3D IC Chiplet Design with Advanced Packaging

- Large-capacity EM solver to enable multi-die 2.5D/3D IC SI/PI analysis
- High-Speed Memory I/O Path: a large number of transmission lines on meshed ground plane need accurate and unified extraction for signal integrity.
- High-Speed Serial I/O Path: accurate TSV model is critical for signal integrity.
- Complex PDN Return Path: a large number of TSVs and DTCs are involved in simulation.



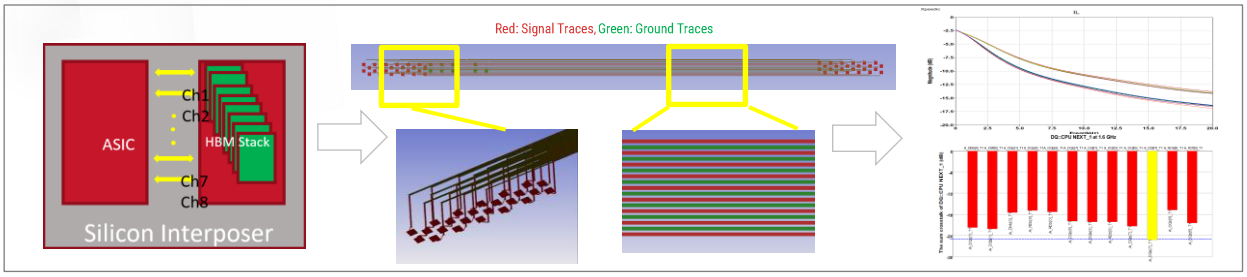
Pre-Layout Modeling and Simulation for RDL and Silicon Interposer

- Metis provides a 2D Interposer template to help users fast create RDL interposer design patterns for quick IL/RL/Xtalk evaluation.
- With the advanced silicon interposer pre-layout template, users can create RDL design patterns for CoWoS-S, and consider both trace and via characteristics for signal integrity.

Result	Structure	1um	1.25um	1.5um	1.75um	2um
VTF Loss		Pass	Pass	Pass	Pass	Pass
VTF Crosstalk		Pass	Pass	Pass	Pass	Pass
VTF Loss		Fail	Fail	Pass	Pass	Pass
VTF Crosstalk		Pass	Pass	Pass	Pass	Pass
VTF Loss		Fail	Fail	Fail	Pass	Pass
VTF Crosstalk		Pass	Fail	Fail	Pass	Pass

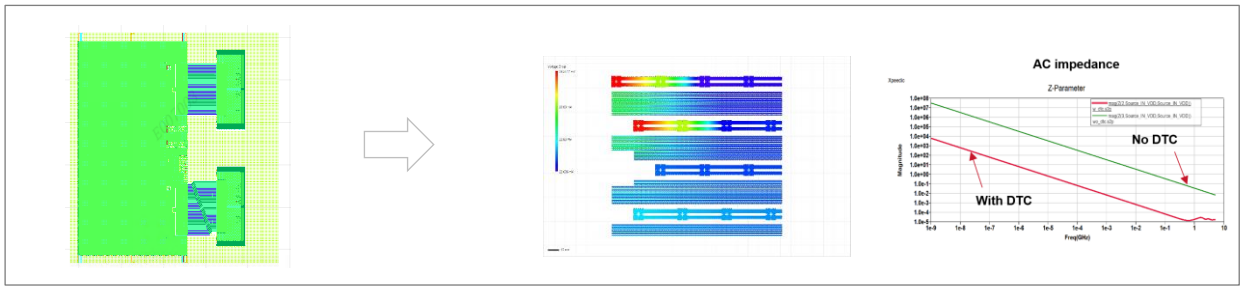
Interposer Signal Integrity Analysis

HBM signals are transmitted between ASIC die and HBM stack. Metis enables users to achieve interposer modeling by wizard for users to simulate channel's loss and crosstalk between different dies accurately.



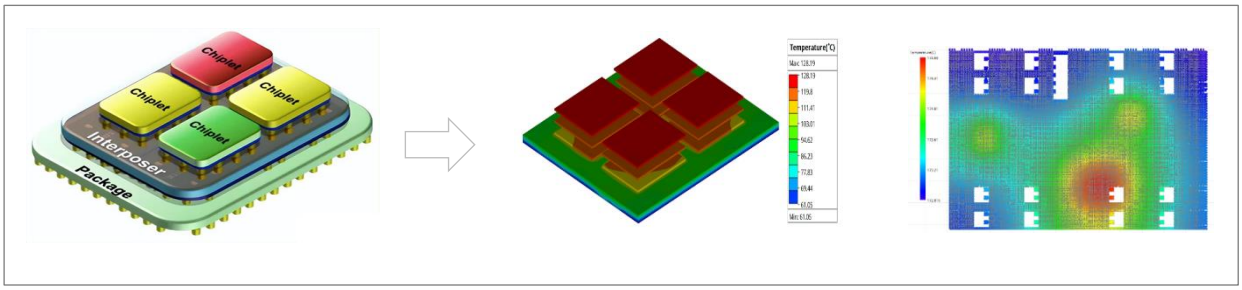
Interposer PDN Analysis

On the silicon interposer, significant numbers of I/O are integrated and they tend to operate at the same time, which will lead to severe simultaneous switching noise (SSN). The performance of system can be heavily degraded when SSN occurs. The analysis of power distribution network (PDN) impedance and DC drop of Chiplet/interposer is a must since it generally affects power supply to the chips as well as signal integrity (SI).



3DIC Thermal Analysis

3D IC vertical stacking enables high integration and superior performance, yet brings severe thermal issues. High power density, stacked dies, dense TSVs and bonding structures create huge thermal resistance, causing heat accumulation and localized hotspots. This leads to performance degradation, thermal stress and reduced chip reliability. Precise early-stage thermal simulation is critical to optimize designs and mitigate thermal risks.



XAI Copilot

XAI Copilot supports natural language input based on local large language models to execute automated SI/PI simulations.